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ELEKTOR ELECTRONICS

THE INTERNATIONAL
ELECTRONICS MAGAZINE

Monochrome VGA adaptor

RADIO DATA SYSTEM DECODER
with clock /alarm function

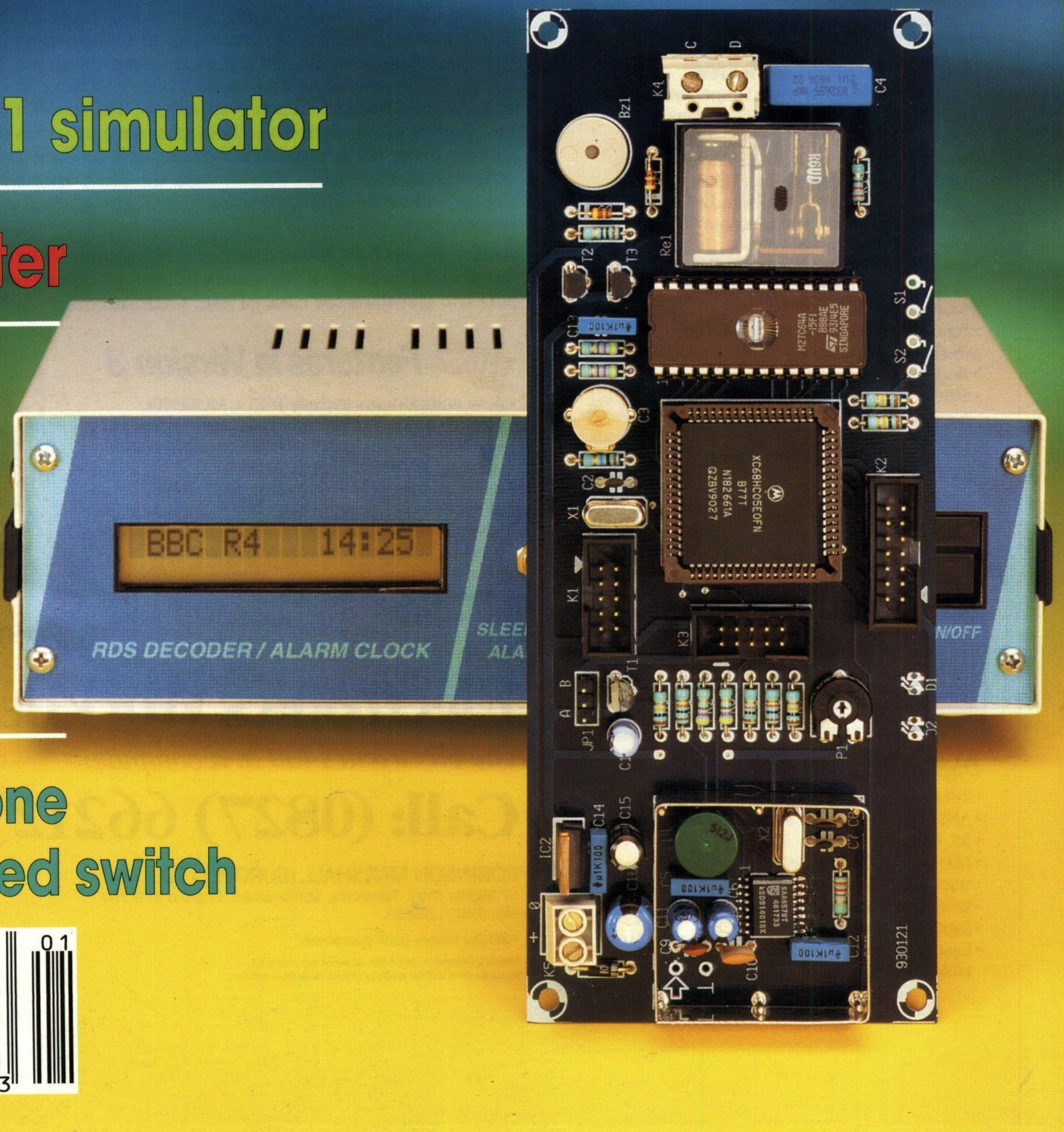
SIM-
an 8051 simulator

I²C tester

Coding for GSM

Digital dial

Telephone controlled switch



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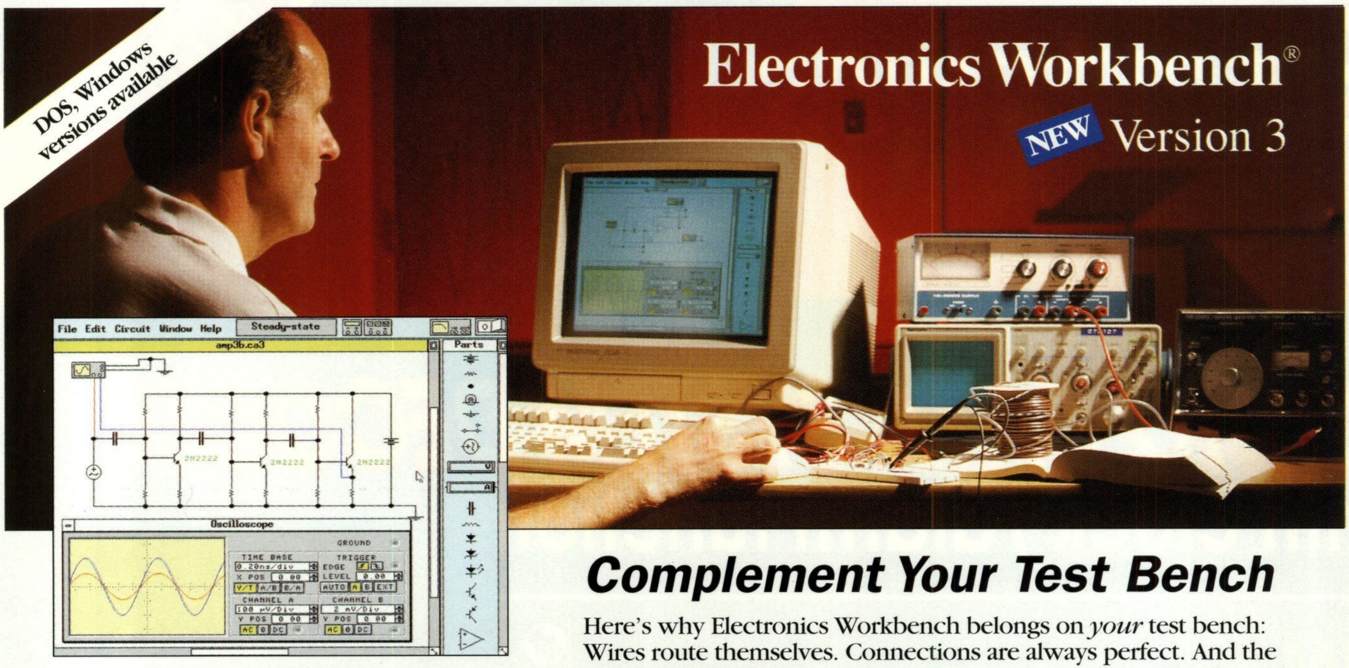

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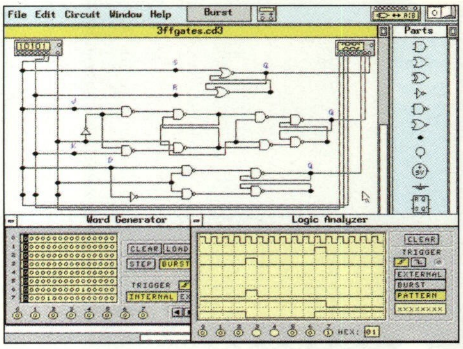

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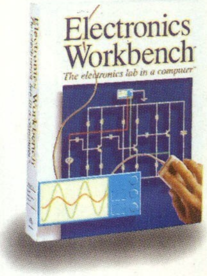

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INTERACTIVE

ELEKTOR ELECTRONICS

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Volume 20
Number 218
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- Building your own toroid core inductors and r.f. transformers
- DAT copybit eliminator
- and others for your continued interest

*We regret that these articles, owing to circumstances beyond our control, could not be placed in the present issue.

Front cover
The Radio Data System (RDS) decoder shown in the photograph and described on pages 24–31 is based on two powerful, yet affordable, ICs: the Philips Components SAA6579T RDS demodulator and the Motorola MC68HC05E0 microprocessor.

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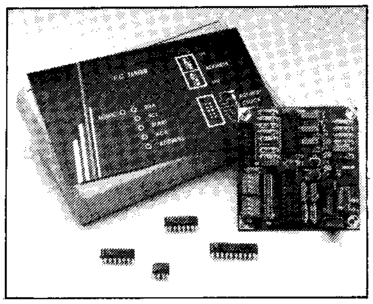

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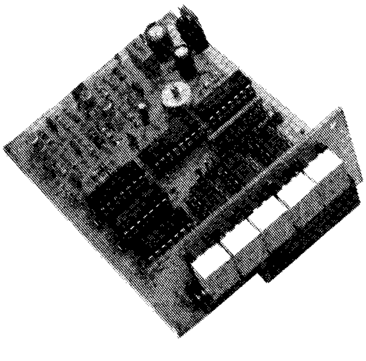

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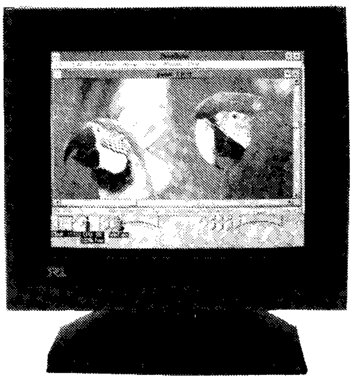

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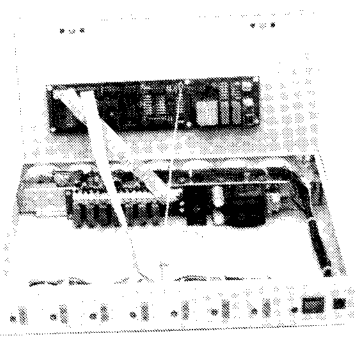

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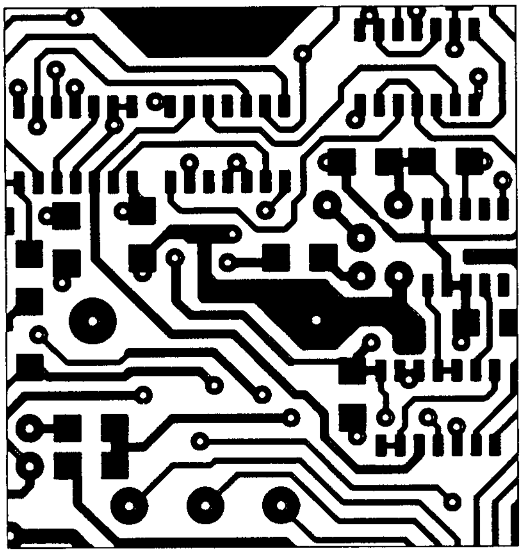

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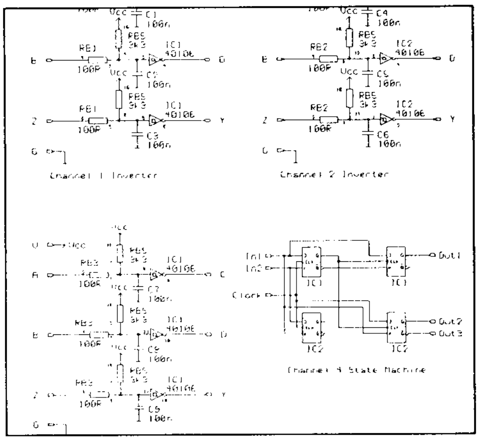

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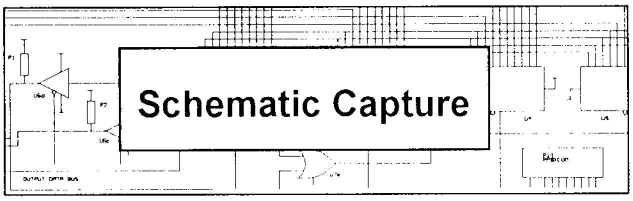

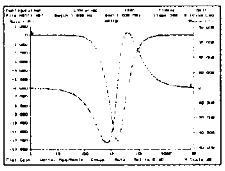

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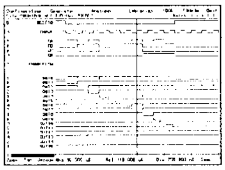

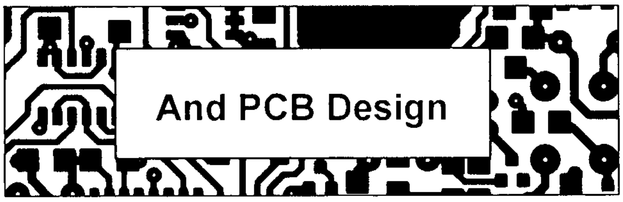

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ELECTRONICS SCENE

BRITISH COMPUTER SKILLS ANIMATE FILM DINOSAURS

By Nigel Hawkes

The successful film *Jurassic Park*, made by the Hollywood director, Mr Steven Spielberg, owes a surprising debt to a small British company tucked away in a London side street. With the help of computer software written by Parallax, launched just three years ago, the animators who worked on *Jurassic Park* have achieved a movie breakthrough weaving seamlessly together sequences filmed in the conventional way with animations created entirely on the computer screen.The result sets new standards in film special effects and opens a Pandorra's box full of tricks for film-makers to exploit.

Traditionally, monster movies since *The Lost World* of 1925 have relied on models to achieve their effects. In *King Kong*, the 1933 classic, in which a giant ape seizes Fay Wray in a hairy embrace and shakes her over the Empire State Building, animator Willis O'Brien painted his scenery on glass sheets mounted on a table, and manipulated a model King Kong frame by frame, creating an illusion of depth and movement. The results, exciting as they were, would not satisfy a modern audience.

Animated models. For *Jurassic Park*, Spielberg started out in the traditional way, commissioning some magnificent dinosaur models from Hollywood specialists. For longer shots, he intended to use animated models in the King Kong style, but his mind was changed by Steve Williams of Industrial Light and Magic, an animation company set up in California in 1975 by George Lucas to make special effects for *Star Wars*. Williams buried himself in his subterranean office and in two weeks created on a computer an animated 10 seconds sequence of a Tyrannosaurus Rex thundering across the screen. Spielberg was hooked.

What has made realistic computer animation possible is the development of high-power workstations with crisp, full-colour graphics, and the software to run them. The terminals are the products of Silicon Graphics, an American company, and cost around £20 000 each. The software, which retails at the same figure, is called Matador and was written in London's Soho by a group of young British programmers working for Parallax.

Sophisticated chips. Parallax is just one of a number of British companies making a success of computer-based entertainment. Argonaut Software, established 10 years ago in North London to produce computer games, now employs 60 people. It hopes to double the 1993 turnover of £4 million in 1994. As well as writing the software for a range of games, the company has developed hardware in the form of sophisticated chips for computer games.

Another London company making a success in the computer game business is BITS, based in Cricklewood, which has so far developed 24 different games for Nintendo and Sega. The firm, started by Foo Katan, employs 35 animators, artists and programmers full-time, plus another 15 who work from home, developing games that are named mostly after current films.

Valuable skills. Gary Shinewald, development director of BITS, believes he knows why British programmers are so good. "Most of us started as schoolchildren in the days of the first home computers, which were not very powerful. So, we had to work hard to get anything worthwhile out of them. Then, when the more powerful Sega and Nintendo machines came along, those skills turned out to be very valueable".

Parallax is a relative newcomer, but in an industry like computing what matters is not age or experience, but what you can deliver. Film companies are convinced that Matador is the right software for them. More than 400 clients, including television companies and leading film studios, now use the program.

The program has already been used in more than 10 major feature films, including the Oscar-winning special effects in *Death Becomes Her*, where Meryl Streep's head was rotated on her body in one stomach-turning sequence, *Cliffhanger* and *The Last Action Hero*. But, by general consent, *Jurassic Park* sets new standards in uniting animation and film.

Wire-mesh image. The animators who worked on the film used 15 separate computer terminals, and each was responsible for a short sequence which were then married together. The process begins with the animator creating on screen the outline of a dinosaur in the form of an open wire-mesh image.

The work is done by drawing with a pencil-like tool on a sloping 'tablet', like a desk-top, which picks up the movements of the pencil and transfers them into the computer as digital signals. At the same time, they appear on a screen. Matador provides the animator with a palette of 16.7 million different hues and a range of special 'brushes' for creating life-like effects such as a smear of mud on a dinosaur's back.

The system also allows an animated sequence to be prepared with much less labour than traditional methods. Films run at 24 frames a second, so the first cartoons were created by drawing a sequence of images of a cartoon character like Felix the cat, each successive image moving on fractionally.

Fewer drawings. Filmed frame-by-frame and then assembled as a sequence, the eye sees the result as a smooth movement. Matador simplifies the process by interpolating between the cartoonist's images, so that he no longer has to draw them all. This reduces the number of drawings he must do by a factor of 10, but against that he must set the fact that the dinosaurs in *Jurassic Park* are realistic creatures, not cartoon characters.

The system then allows the computer-created sequences to be integrated with earlier filmed shots in which the actors performed in empty space, imagining the dinosaurs. Images are digitized and fed into the computer, where they can be combined electronically with the animated sequences. Finally, the combined images are turned back into film.

The results impressed both the animators at Industrial Light and Magic and Steven Spielberg himself. With the skin of the dinosaurs moving and their bellies swaying, there is not much danger of modern youngsters complaining they are not real enough.

Powerful techniques. There is a danger, however, Steve Williams believes, that the new techniques are so powerful that they may one day be used to manipulate history. Old archive films have a peculiar power because we know they tell the truth: the camera, as the saying goes, can not lie. But soon, it will be posible to remodel these images in the computer, creating, say, bogus films. The power of computer graphics will eventually allow the use of computer-generated presidents who have been dead for some time giving a speech. When you are looking at the television, you won't know what is real and what is not.

DEVELOPERS' KIT FOR PHILIPS 87C750 MICROCONTROLLER

Developers working with the Philips 87C750 microcontroller can now get a low-cost, feature-packed tool set in a new software development kit available from Micro AMPS.

Included with the 87C750-SDK kit is MICRO/EDITOR, a full-featured, multi-window text editor, MICRO/ASM-750, a robust Macro Assembler,and MICRO/SLD-750, a simulator/Source Language Debugger. This DOS-based development package has been configured especially to support an 87C750 Target Processor Environment, including memory spaces and peripheral ports and timers. Also supported is a Source Debug Environment including instruction single step, breakpoints, watch windows and over 17 additional tools.

Applications for the 87C750 include consumer and industrial products that can benefit from its 80C51 architecture, small package size and low cost.

The87C750-SDK is available at an introductory price of £49·95 until April this year. The regular list price is £125. For more information, contact **Micro AMPS Ltd, 66 Smithbrook Kilns, Cranleigh, Surrey GU6 8JJ. Telephone +44 (0)483 268 999; Fax +44 (0)483 268 397.**

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Papers should be submitted by 7 January, 1994, to the **ADDA 94 Secretariat, IEE Conference Services, Savoy Place, London WC2R 0BL. Telephone 071 344 5478/5477, fax 071 497 3633**, from whom details are available.

HOW TO PROGRAM TOSHIBA MICROS

Lloyd Research has produced a practical solution to an old problem: how to program low-cost micros such as the Toshiba TMP47PC242VN. After a design is complete, it is usually necessary to use OTP parts until the desighn is finally proved and mask parts are available. In addition, with the lowering of costs of OTP parts, many companies are not using mask parts at all.

A simple solution is to buy a number of single socket adaptors and to use a standard EPROM programmer. Such adaptors are usually wider than a single socket on the programmer, so it is rarely possible to fit more than four sockets on an eight-gang programmer. In addition, the programmer may need to be set up each time for a different address range. As if this is not enough, there is always the problem of the mechanical fit of a delicate adaptor in a production environment.

Lloyd Research has overcome this problem by designing a special module for their L9000 programmer. The PL242 module is fited with four sockets for shrink dip devices. A second identical or different module can be fitted to double the capacity or to program other devices such as EPROMs or other microcontrollers.

To cater for short-term requirement, programming systems can be rented from Lloyd Research.

The L9000 is made and supported in the UK by Lloyd Research who have been making programmer for ten years. Production managers can also take comfort from approvals the company has received from Intel, Texas Instruments and Signetics.

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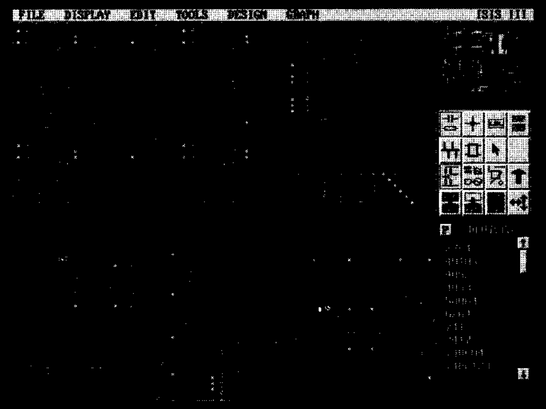

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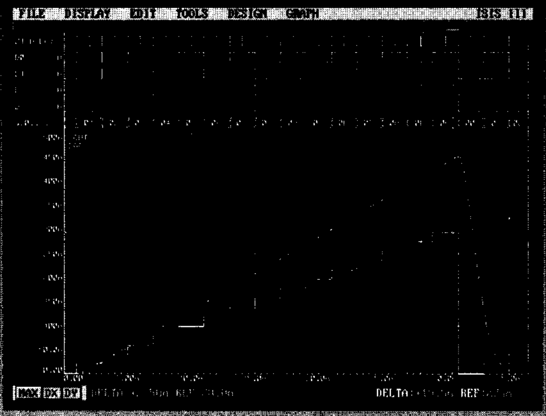

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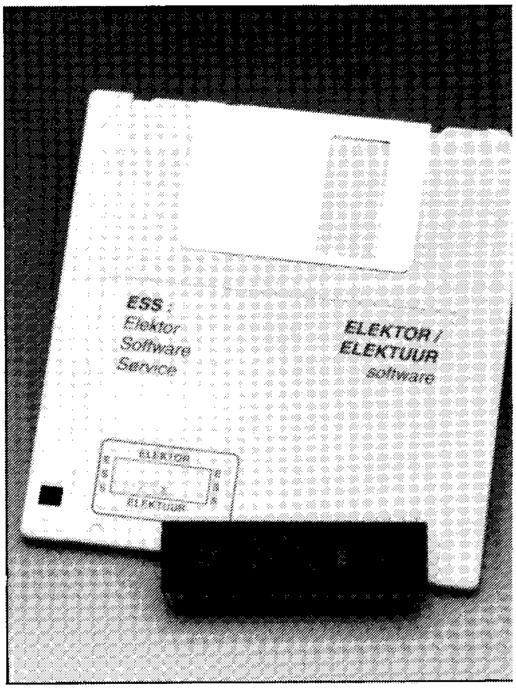
SIM — AN 8051 SIMULATOR

This article describes how to use SIM, a power-packed program that simulates an 8051 microcontroller on an IBM PC, providing a perfect complement to the 8051/8032 assembler course which so many of you have followed with great interest. The reasons for using a simulator are given, followed by a brief description of SIM's facilities. A short program is used to demonstrate how to use the simulator, with commentary on how each feature is used for program development and debugging. Finally, a typical program bug is demonstrated.



By David Mockridge

WHEN programming a microcontroller like the 8051, the development environment is Spartan. Development tools are often command-line oriented or run only with dedicated ICE (In-Circuit-Emulator) hardware. Although an ICE is an excellent solution for embedded system developers, it is expensive.

On the other hand, those who program in high-level languages work in comparative luxury. When things go wrong in Basic, C or Pascal, all they need do is single-step through the code with a fly-swatter at the ready. A host of powerful features are available, such as setting watches on variables, editing data and breakpoints.

The microcontroller programmer with a smaller budget has access to none of these facilities. After the program has been written, assembled and burnt to EPROM (or downloaded to an emulator), the programmer is often left staring in frustration at a smug lump of silicon, wishing the lid could be taken off with a screwdriver to see what is happening inside. (A heavy blunt object will open the chip quite effectively, but re-assembly is tricky.)

When confronted with this problem, the embedded-system designer may turn to the fifteen or so vendors of 8051 development software. This route is still expensive, even if the often compulsory additional hardware is avoided. SIM provides a solution.

SIM in a nutshell

SIM is a program that simulates an 8051 microcontroller. It runs on an IBM or IBM-compatible PC without any dedicated hardware. SIM will run your program either continuously or by single stepping one instruction at a time. Like high-level language environments, you can set watches to see the contents of any register, port or on-chip RAM location while the program is executing. If the system being developed uses an external RAM, its data can be watched, too. All registers and both of the RAM areas may be edited at any time. Breakpoints can be set to halt the simulator at selected addresses, so that the state of the machine can be examined. Breakpoints and watches are dynamically manipulated with a window-based menuing system. Context-sensitive on-line help is provided for all simulator functions, as well as help for all 8051 instructions. The disassembled mnemonics displayed by the simulator are Intel-compatible. SIM comes with a command-line disassembler and assembler.

Start, Reset and Run

The short program in **Fig. 1** will be used to demonstrate how SIM works.

```
SNAIL Tiny Assembler, at 22:40:19 on 09-06-1993.  Source: "EX_1.ASM"
---------------------------------------------------------------------

               1    ; SIM DEMONSTRATION PROGRAM EX_1
               2    ; FLASHES AN LED ON PORT 1 BIT 0
               3
               4    ; EQUATES
               5    LED_1 EQU 90H
               6
0000           7    START:
0000 74FF      8      MOV A,#FFH ; LOAD ACCUM. WITH DELAY CONSTANT
               9
0002          10    CONTINUE:
0002 14       11      DEC A       ; SUBTRACT 1 FROM THE ACCUMULATOR
0003 FD       12      MOV R5,A    ; MOVE ACCUMULATOR TO REGISTER 5
0004 00       13      NOP         ; NO OPERATION, DO NOTHING
0005 70FB     14      JNZ CONTINUE ; DOWN TO ZERO YET?
0007 110B     15      ACALL TOGGLE_LED ; CALL FLIP LED ROUTINE
0009 80F5     16      SJMP START
              17
000B          18    TOGGLE_LED:
000B B290     19      CPL LED_1    ; COMPLEMENT (= INVERT) LED BIT
000D 22       20      RET          ; RETURN FROM SUBROUTINE
              21
              22

Statistics after assembly    (22:40:20 09-06-1993)
-------------------------
Found 1 equate:
  1: ........... "LED_1" equates to "90H"

Found 3 labels:
  1: ........... "START" was at address 0H
  2: ........ "CONTINUE" was at address 2H
  3: ....... "TOGGLE_LED" was at address BH

 14 Bytes of object code were written. (0H..DH)

Source file: EX_1.ASM      List file: EX_1.LST      Object file: EX_1.OBJ
 1561 Bytes of listing file were generated.
```

Fig. 1. LST (list) file produced by asembling EX_1.ASM.

While symbolic names are shown in the assembly listing, SIM disassembles the raw object file, and will not display these. Start the simulator by typing 'SIM' at the DOS command line. Select the menu bar 'File' option by typing 'F', followed by the filename 'EX_1.OBJ'. As SIM loads this file, it will display a screen of disassembled instructions, with a highlight bar over the next instruction to be executed, which will be 'CLR A' (clear accumulator).

Once the file is loaded, single-step through the code one instruction at a time by pressing 'S' repeatedly, or run continuously by pressing 'N' for the menu 'Run' option. Once you have tried both methods out (use the space bar to stop running), type 'R' to reset. This option performs a CPU reset of the simulator (not the PC!). When your program jumps into uncharted address space (outside your program area), the simulator will not budge until it is reset in this way. After your CPU reset, notice that the highlight bar has returned to address 00.

Now type 'B' to select the Breakpoints option. Menu options in windows like these are selected by moving the highlight bar over your choice with the arrow keys, followed by the enter key. Select 'Add breakpoint', then enter '5' to set a breakpoint at this address. Now that a breakpoint has been set, when you set SIM running, it will only go as far as address 5, where it will wait for you to single-step or run further onwards. Breakpoints have no effect when single-stepping, since you stop on every instruction anyway. Breakpoints are invaluable when you want to debug portions of program code that can only be properly tested by running through initial processing. When initial processing is unnecessary for testing, then the 'Goto' option may be used. The 'Clear all' option on the breakpoints menu will remove all breakpoints, irrespective of how many are set. If you want to set a breakpoint at your current location (wherever the highlight bar is located), you can use the 'Set Brkpt here' menu option. Breakpoints (like edit quantities and goto addresses) are always entered in hexadecimal. Use 'List breakpoints' to review the breakpoints that have been set, and 'Delete breakpoints' to remove them individually.

Adding a watch

Next we will add a watch so we can see what is happening inside the accumulator. Choose the 'Watch' menu from the menu bar with 'W'. Select 'Add watch' followed by 'SFRs / CPU'. All the SFR (Special Function Registers) in the 8051 are displayed in this window (see **Fig. 2**). The cursor will be parked on the accumulator ('A') register by default. When you move over other registers (use the arrow keys), you will see the direct address of each one displayed at the upper right of the window. Return your selection to the accumulator, and press Enter. Select the first binary format ('Binary 1') to watch the accumulator in binary. You can set several watches on the same piece of data using different formats for each one. For example, if you want to watch the accumulator in hexadecimal as well as in binary, all you need to do is repeat the previous actions, only selecting the format 'Watch as hex' instead of 'Binary 1'.

SIM SYSTEM REQUIREMENTS

IBM or IBM compatible PC, 640 K RAM, monochrome or EGA or better screen adaptor. DOS 3.2 or later.

Choose the 'Default name' option for now. When you hit Enter, the accumulator will appear in the watch window.

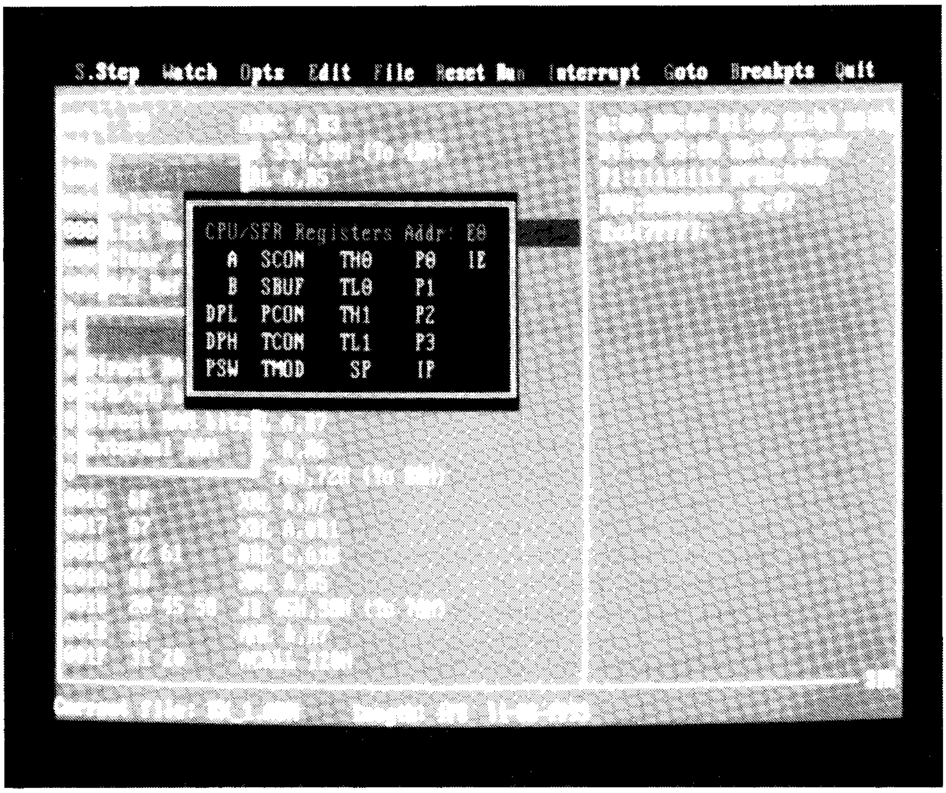
If you single-step or run through the program at this stage, you will be able to see inside the accumulator as it is changed by the program.

The 'New name' option in the add watch menu allows you to enter your own names for watched data. For instance, if you had a DIP-switch attached to a port, you might prefer to name the port 'DIP switch' instead of using the default watch name of 'P1'. In a timer program, you may want to name an on-chip RAM location or register as 'Seconds count' instead of using an address. Another add watch option 'Join with prev' allows you to string watched pieces of data together by omitting the text descriptor adjacent to the watch data. Since watches are byte-oriented, this allows you to watch a set of (not necessarily contiguous) bytes as if they were a string.

Now that you have added a watch on the accumulator, try adding a watch on R5 (register 5), which is at direct address 5. Select 'Add watch', then the 'Direct RAM' option. Specify address 5 for register five in address bank zero, and type in 'R5' for the 'New name' option. If you add the stack pointer too (SFR/CPU window register SP), you can now watch the accumulator, stack pointer and register 5. Notice how the stack pointer goes up by two as the source address is pushed on to the stack, every time the subroutine call at address 7 is made. It falls correspondingly by two whenever the return address is popped off by the subroutine return instruction.

Default watches

There is a special watch option to add a convenient default set of watches at once. These consist of the accumulator, registers 0 to 7 (from register bank 0), the data pointer (DPTR), port 1, the program status word (PSW) and the stack pointer. To do this, select the 'Add default' watch menu option. The



```
CPU/SFR Registers Addr: E0
  A  SCON   TH0   P0  IE
  B  SBUF   TL0   P1
DPL  PCON   TH1   P2
DPH  TCON   TL1   P3
PSW  TMOD    SP   IP
```

Fig. 2. The Watch menu enables you to peek inside the 8051, and see what is happening to the SFRs and the CPU.

```
SNAIL Tiny Assembler, at 22:37:06 on 09-06-1993.  Source: "EX_2.ASM"
-------------------------------------------------------------------

               1    ; SIM DEMONSTRATION PROGRAM EX_2
               2    ; FLASHES AN LED ON PORT 1 BIT 0
               3    ; BUT USE A NESTED LOOP TO MAKE FLASHING
               4    ; SLOW ENOUGH TO BE VISIBLE.
               5
               6    ; EQUATES
               7    LED_1      EQU  90H
               8    TIMEDLY1  EQU  #FFH
               9    TIMEDLY2  EQU  #FAH
              10
0000          11    CARRYON:
0000 1109     12      ACALL DELAY        ; LONG DELAY SUBROUTINE
0002 1106     13      ACALL TOGGLE_LED  ; FLIP LED SUBROUTINE
0004 80FA     14      SJMP CARRYON       ; DO THIS ENDLESSLY
              15
              16    ; SUBROUTINE TO TOGGLE THE STATE OF LED BIT
0006          17    TOGGLE_LED:
0006 B290     18      CPL LED_1    ; COMPLEMENT (= INVERT) LED BIT
0008 22       19      RET          ; RETURN FROM SUBROUTINE
              20
              21    ; SUBROUTINE FOR LONG DELAY
0009          22    DELAY:
0009 78FF     23      MOV R0,TIMEDLY1  ; PRIME OUTER LOOP
              24
000B          25      FINISHEDYET?:
000B E8       26      MOV A,R0          ; CHECK IF OUTER LOOP DELAY DONE
000C 600C     27      JZ DONEDELAYING  ; GET OUT IF IT IS
000E 74FA     28      MOV A,TIMEDLY2   ; ELSE START ANOTHER INNER LOOP
              29
0010          30        INNERLOOP:
0010 00       31        NOP             ; DO NOTHING TO INCREASE DELAY
0011 00       32        NOP
0012 00       33        NOP
0013 00       34        NOP
0014 D5E0F9   35        DJNZ E0H,INNERLOOP ; E0H IS ACCUMULATOR DIRECT
              36
0017 18       37      DEC R0
0018 80F1     38      SJMP FINISHEDYET?
              39
001A          40      DONEDELAYING:
001A 22       41      RET
              42
              43

Statistics after assembly    (22:37:09 09-06-1993)
------------------------
Found 3 equates:
  1: ........... "LED_1" equates to "90H"
  2: ........ "TIMEDLY1" equates to "#FFH"
  3: ........ "TIMEDLY2" equates to "#FAH"

Found 6 labels:
  1: ......... "CARRYON" was at address 0H
  2: ....... "TOGGLE_LED" was at address 6H
  3: ........... "DELAY" was at address 9H
  4: ..... "FINISHEDYET?" was at address BH
  5: ........ "INNERLOOP" was at address 10H
  6: ..... "DONEDELAYING" was at address 1AH

 27 Bytes of object code were written. (0H..1AH)

 Source file: EX_2.ASM     List file: EX_2.LST     Object file: EX_2.OBJ
  2727 Bytes of listing file were generated.
```

Fig. 3. LST (listing) file of EX_2, an example program that flashes a LED at a visible rate.

results of this action are shown in **Fig. 2**. Since maintaining a large number of watches can slow the simulator down, you may wish to delete some watches. Do this by selecting the 'Delete' option from the watches menu. Page up and down through the list if necessary, until you have placed the highlight bar over the watch to be deleted. Press Enter to delete the selected watch, and use the Escape key to quit out when you have finished deleting. Use the 'List' watches option to review the watches set without deleting any. The list, delete and add functions of the breakpoints menu are operated in exactly the same way.

Goto, Help and Escape

The 'Goto' option will allow you to start executing from any address in your program. If you go to a data address, the simulator will interpret the data as an instruction, with unwanted results. Use the Goto option with care, although if you do get lost by branching into a data area by mistake, you can always reset and start over. To practice a Goto command, do a reset, select menu option 'Goto' and enter address 7, the address of the subroutine call. The highlight bar will jump to address 7, from where you can now single-step (or run). 'Goto' is useful for skipping past portions of code that you know are working, and for testing subroutines in isolation.

Wherever you go in the menu system, context-sensitive help is at hand. Select the watch menu again, and make a few random choices. Press F1 to pop up the help window, followed by Enter again to get context-sensitive help for the watch sub-menu you are at. When you have finished reading, use the Escape key to quit out of help. Pressing Escape repeatedly will back you up through the sub-menu windows chosen up to this point. Another option in the help window provides help for each op code in the 8051's instruction set. The help descriptions are no substitute for trying the instructions out with the simulator, which is more fun than merely reading about them.

A bit at a time

The 8051 has a dedicated Boolean bit processor and accompanying bit-oriented instructions. SIM allows you to set watches on bits and edit them individually. Add a watch as before, but select the 'SFRs/CPU bits' option to see a window with all bit-addressable registers and their bits (also shown in Fig. 2). When the bits have special names, for example CPU flags, these are shown. The bits covered with asterisks which the cursor skips are not bit addressable. Besides the SFR bits, all the directly addressable bits in the chip are individually selectable in a special window for single-bit editing and watching. Watches may be set on individual bits of ordinary direct RAM, but these may only be edited at a byte level. Try setting a watch on port 1 bit 0, and then use 'Edit' to change its value before the program does. The watch window is updated immediately as you complete the edit. Editing can be used to simulate external events like switch depressions or A/D (analogue-to-digital) inputs, by setting data at ports.

Another use for editing is escaping from a loop (or nested loops) that rely on a counter reaching a particular value before moving on. In the test program, we have to wait for the simulator to count down from 255 (FF_H). Once the loop has been entered, this longish wait can easily be cut short by editing the accumulator down to a few cycles away from completion.

Interrupts

The interrupt menu lets you choose a hardware interrupt to trigger. Like the

```
      ; Stack-destructing demonstration
      Start:
         ACALL SubroutineOne
      SubroutineOne:
         SJMP Start




SNAIL Tiny Assembler, at 22:41:29 on 09-06-1993.  Source: "EX_3.ASM"
---------------------------------------------------------------------

              1    ; STACK-DESTRUCTING DEMONSTRATION
0000          2    START:
0000 1102     3       ACALL SUBROUTINEONE
0002          4    SUBROUTINEONE:
0002 80FC     5       SJMP START
              6

Statistics after assembly    (22:41:29 09-06-1993)
-------------------------
No EQU(ate) statements were found in this source file.

Found 2 labels:
  1: ........... "START" was at address 0H
  2: .... "SUBROUTINEONE" was at address 2H

 4 Bytes of object code were written. (0H..3H)

Source file: EX_3.ASM      List file: EX_3.LST      Object file: EX_3.OBJ
 773 Bytes of listing file were generated.
```

Fig. 4. Assembler (ASM) and listing (LST) file of a stack-destructing program, EX_3.

physical 8051, interrupts are ignored unless they are properly enabled with the interrupt priority register. SIM also traps attempts to vector to an interrupt past the end of your program, and displays a warning. Try a serial port interrupt (interrupts menu, option 'R1 & T1') to do this intentionally. Do not forget that whenever you are confronted with a warning message box like this, you can always use help to get more details on the condition that caused it.

The tiny demonstration program was chosen for size and simplicity. With a 16-MHz clock the flash rate is invisibly fast. See the program 'EX_2.LST' in **Fig. 3** for a nested-loop flasher that is slower, and which flashes visibly. While each example program fits on one screen, SIM handles programs that span several screens, displaying only the current screen. When a jump is made off the screen, a new screen is disassembled from the destination address onwards.

Catching a bug

The program in **Fig. 4** demonstrates an interesting bug. A subroutine call is made repeatedly without ever executing a return. One would expect the stack pointer to wrap around (SIM will trap this event and issue a warning), but it does not. The stack pointer itself is located at address 81_H, above the top of the stack. This means it points to itself when it grows too high, writing pushed address data over the pointer before it grows higher still. The fault is obvious in such a tiny program, but a larger program might well have the same problem, only buried in hundreds or thousands of lines of code.

Try loading and running program 'EX_3.OBJ', to see it self-destruct. The results make it clear how important it is to return from subroutines.

External RAM consists of RAM chips physically external to the CPU. Since external RAM can take up 64 KBytes memory, SIM only allocates storage for external memory if it is referenced. When any action (edit, watch or move) is performed on an external memory location, that location is created and maintained by SIM. This approach saves memory space but imposes an increasing processing time overhead if many external memory locations are used. SIM is not recommended for programs needing large amounts of external memory.

Object file edit facility

SIM incorporates a file edit function. This facility allows changes to be made to the file you are running in the simulator, without exitting SIM. Instead of quitting, changing your assembler source code, reassembling it and then starting the simulator again (assuming you had no assembly errors), the file edit facility allows you to change values in the object file you are running, while you are running it. If you change an instruction displayed on-screen, the screen will be re-disassembled to reflect your change. Changes may be made to any instruction or data, including the highlighted (next to be executed) instruction. This does mean that your assembly source code is no longer in step, but fresh source code can be generated by running your changed object file through the disassembler. The disassembled code will not, of course have any comments or labels in it, so changing your assembler source will usually be a better option.

SNAIL, DISASS and SIM

All example programs referred to in this article are provided with SIM, in source and compiled form. A tiny but fully-functional 8051 assembler called SNAIL is provided with SIM for those who have not yet got one. SNAIL and DISASS are limited to small (around 15 KBytes maximum) source files. DISASS is a full 8051 disassembler, useful for picking up bugs. DISASS comes with SIM. Brief documentation and sample programs for the disassembler, assembler and simulator are provided on the diskette. Add your favourite editor or word processor, and you have all the tools required to develop 8051 programs.

The example programs used here were the simplest possible demonstrations. SIM is capable of much more, including responding to software interrupts, register bank switching, power-down modes, relative address decoding, running object files of up to 65 K and use of the full instruction set.

Finally I would like to mention the little-known software design phase known as bugging. This occurs somewhere between the design and coding stages, and is inversely proportional to the time required for the better known phase of debugging. Cutting down on bugging time is difficult, but by using SIM I hope you will lessen debugging time considerably. ■

For further reading:

8051/8032 assembler course (8 instalments), *Elektor Electronics* February through November 1992.

Program ordering information

The programs SIM, SNAIL, DISASS, explanatory text files, and the three example files discussed here are contained on a single 3½-inch MSDOS formatted diskette which may be ordered through the *Elektor Electronics* Readers Services. The order code is **1931**. Price and ordering details may be found on page 70.

The courseware diskette and the system monitor EPROM for the *8051/8032 Assembler Course* are also available through the Readers Services. The order code is **1661**.

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4009AE	0.23
4009UB	0.29
4010B	0.29
4011B	0.18
4011UB	0.18
4012AE	0.16
4012B	0.20
4013B	0.20
4014B	0.42
4015B	0.42
4016B	0.24
4017B	0.38
4018B	0.38
4019B	0.26
4020AE	0.36
4020B	0.38
4021B	0.40
4022B	0.40
4023B	0.20
4023UB	0.23
4024AE	0.27
4024B	0.32
4025B	0.19
4026B	0.54
4027B	0.30
4028B	0.38
4029B	0.35
4030B	0.21
4031B	1.04
4032B	0.70
4033B	0.58
4034B	1.10
4035B	0.39
4036B	2.57
4037B	1.27
4038B	0.78
4039B	3.22
4040B	0.42
4041B	0.41
4041UB	0.32
4042B	0.32
4043B	0.36
4044B	0.36
4045B	0.94
4046B	0.42
4047B	0.38
4048B	0.82
4049B	0.24
4049UB	0.28
4050B	0.22
4051B	0.34
4052B	0.33
4053B	0.34
4054B	0.68
4055B	0.62
4056B	0.48
4059B	2.98
4060B	0.38
4063B	0.42
4066B	0.27
4067B	1.85
4068B	0.20
4069UB	0.21
4070B	0.21
4071B	0.20
4072B	0.20
4073B	0.20
4075B	0.19
4076B	0.42
4077B	0.20
4078B	0.21
4081B	0.18
4082B	0.20
4085B	0.38
4086B	0.38
4089B	0.98
4093B	0.24
4094B	0.38
4095B	0.70
4096B	1.10
4097B	2.75
4098B	0.40
4099B	0.42
4104P	1.01
4160B	0.85
4161B	0.85
4174B	1.27
4175B	1.14
4194B	1.43
4409P	11.05
4410P	16.45
4411P	21.58
4412FP	POA
4412FL	POA
4412VP	POA
4416P	POA
4419P	POA
4429PB	POA
4433P	POA
4443P	POA
4447P	POA
4468P	POA
4469P	POA
4489P	POA
4490P	3.20
4495P	6.27
4497P	13.58
4499P	6.24
4500B	19.45
4501B	0.32
4502B	0.38
4503B	0.38
4504B	1.12
4505B	4.42
4506B	1.14
4506U	1.14
4508B	1.14
4510B	0.54
4511B	0.44
4512B	0.38
4513B	1.20
4514B	1.12
4515B	1.12
4516B	0.44
4517B	1.84
4518B	0.40
4519B	0.36
4520B	0.36
4521B	0.72
4522B	0.86
4526B	0.50
4527B	0.56
4528B	0.49
4529B	0.57
4530B	1.92
4531B	1.14
4532B	0.44
4534B	2.82
4536B	1.22
4538B	0.60
4539B	0.62
4541B	0.52
4543B	0.57
4544B	2.11
4547B	1.68
4549B	POA
4551B	1.62
4553B	2.37
4554B	6.01
4555B	0.48
4556B	0.49
4557B	1.88
4558B	2.18
4560B	1.51
4561B	1.74
4562B	5.15
4566B	1.10
4568B	5.17
4569B	3.04
4572UB	0.70
4573P	POA
4580B	8.84
4581B	3.85
4582B	3.85
4583B	0.86
4584B	0.57
4585B	0.49
4597CP	6.90
4598B	6.90
4599B	5.50
4720B	POA
4720V	POA
4723B	POA
4724B	1.90
4731VP	9.80
4737VP	18.28
4738VP	18.50
4750VD	28.50
4752VP	29.25
4753VP	POA
4754VP	POA
40085	1.98
40097	0.62
40098	0.62
40100	2.48
40101	POA
40102	1.20
40103	0.88
40105	1.82
40106	0.30
40107	0.42
40108	POA
40109	1.24
40110	1.04
40114	2.62
40116	12.48
40117	1.80
40147	1.23
40160	0.54
40161	0.54
40162	0.54
40163	0.54
40174	0.34
40175	0.47
40181	POA
40192	0.62
40193	0.74
40194	1.82
40195	2.24
40240	2.62
40244	1.36
40245	1.36
40257	0.54
40373	1.10
40374	1.10
45026	4.42
45027	5.99
45028	4.49
45040	POA
45041	POA
45100	POA
45106	7.98
45109	POA
45138	POA
45145	10.04
45146	POA
45151	19.50
45152	21.45
45156	15.80
45157	14.38
45158	11.94
45159	POA
45406	2.73
45407	6.47
45411	POA
45414	15.60
45428	POA
45433	POA
45440	POA
45441	POA

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4021BT	0.65
4023BT	0.38
4024BT	0.76
4025BT	0.38
4027BT	0.45
4028BT	0.56
4029BT	0.86
4040BT	0.78
4042BT	0.74
4046BT	1.41
4047BT	1.06
4049BT	1.06
4050BT	0.48
4051BT	0.78
4052BT	0.84
4053BT	0.98
4060BT	0.84
4066BT	0.59
4068BT	0.38
4069UBT	0.38
4070BT	0.38
4071BT	0.38
4075BT	0.38
4077BT	0.38
4078BT	0.38
4081BT	0.38
4093BT	0.45
4094BT	0.95
4508BT	2.05
4510BT	1.02
4511BT	1.35
4512BT	0.68
4514BT	2.20
4516BT	1.02
4518BT	1.18
4520BT	1.18
4521BT	1.07
4522BT	1.22
4528BT	0.88
4534BD	POA
4538BT	1.05
4541BT	1.05
4543BT	1.02
4555BT	POA
4556BT	1.05
4585BT	0.95
40106BT	0.53
40244BT	1.35
40373BT	2.34

74 SERIES

7400	0.36
7401	0.30
7402	0.34
7403	0.34
7404	0.40
7405	0.40
7406	0.68
7406A	0.72
7407	0.63
7407A	0.65
7408	0.37
7409	0.67
7410	0.35
7412	0.64
7413	0.76
7414	0.72
7416	0.53
7417	0.48
7420	0.37
7425	0.59
7426	0.48
7427	0.59
7430	0.35
7432	0.45
7437	0.59
7438	0.49
7440	0.77
7442	0.55
7445	1.20
7446	1.53
7447	0.98
7447A	1.67
7451	0.57
7454	0.72
7470	0.54
7472	0.38
7473	0.59
7474	0.53
7475	0.67
7476	0.72
7480	1.26
7483	1.10
7485	0.58
7486	0.53
7490	0.76
7490A	1.34
7491	2.56
7492	0.67
7492A	1.12
7493	0.68
7493A	0.70
7495A	1.10
7497	5.23
74104	0.67
74107	0.60
74110	POA
74116	3.10
74118	POA
74119	POA
74121	0.98
74123	0.94
74125	0.67
74126	0.98
74128	1.19
74132	0.86
74145	1.16
74150	1.86
74151	0.80
74151A	0.80
74153	0.90
74154	2.16
74155	0.81
74157	0.74
74158	1.57
74159	3.98
74160	0.94
74161A	0.98
74163	1.28
74164	1.20
74165	1.57
74166	1.06
74174	1.53
74175	1.23
74180	1.29
74184	POA
74185	1.76
74191	1.41
74192	1.41
74193	1.65
74221	1.23
74259	2.92
74265	1.46
74273	POA
74276	3.56
74279	1.38
74283	1.26
74298	POA
74365	0.70
74367	1.06
74393	2.94
74403	POA
74423	POA

74LS SERIES

74LS00	0.18
74LS01	0.18
74LS02	0.18
74LS03	0.18
74LS04	0.21
74LS05	0.21
74LS06	0.51
74LS07	0.51
74LS08	0.18
74LS09	0.18
74LS10	0.18
74LS11	0.18
74LS12	0.18
74LS13	0.19
74LS14	0.24
74LS15	0.38
74LS20	0.18
74LS21	0.18
74LS22	0.18
74LS24	0.58
74LS26	0.18
74LS27	0.18
74LS28	0.24
74LS30	0.18
74LS31	1.58
74LS32	0.20
74LS33	0.20
74LS37	0.18
74LS38	0.18
74LS40	0.18
74LS42	0.32
74LS44	2.11
74LS47	0.55
74LS48	0.54
74LS49	1.38
74LS51	0.19
74LS54	0.19
74LS55	0.32
74LS73	0.40
74LS73A	0.48
74LS74	0.22
74LS74A	0.24
74LS75	0.28
74LS76	0.68
74LS76A	0.72
74LS77	0.42
74LS78	0.32
74LS83	0.39
74LS83A	0.39
74LS85	0.38
74LS86	0.27
74LS90	0.40
74LS91	POA
74LS92	POA
74LS93	0.44
74LS95	0.48
74LS96	0.82
74LS107	0.28
74LS107A	0.38
74LS109	0.28
74LS109A	0.32
74LS112	0.28
74LS112A	0.34
74LS113	0.32
74LS113A	0.38
74LS114	0.32
74LS114A	0.36
74LS122	0.39
74LS123	0.36
74LS125	0.28
74LS125A	0.32
74LS126	0.32
74LS126A	0.36
74LS132	0.29
74LS133	0.18
74LS136	0.38
74LS137	0.98
74LS138	0.31
74LS139	0.34
74LS145	0.66
74LS147	2.86
74LS148	0.83
74LS151	0.32
74LS153	0.32
74LS154	1.12
74LS155	0.34
74LS156	0.38
74LS157	0.38
74LS158	0.34
74LS160	0.48
74LS160A	0.54
74LS161	0.46
74LS161A	0.49
74LS162	0.48
74LS162A	1.07
74LS163	0.42
74LS163A	0.47
74LS164	0.34
74LS165	0.59
74LS166	0.59
74LS168	0.75
74LS169	0.59
74LS170	POA
74LS173	0.39
74LS173A	0.44
74LS174	0.36
74LS175	0.34
74LS181	1.82
74LS182	2.05
74LS183	2.05
74LS189	2.60
74LS190	0.49
74LS191	0.49
74LS192	0.49
74LS193	0.48
74LS194	0.54
74LS194A	0.57
74LS195A	0.57
74LS196	0.68
74LS197	0.68
74LS221	0.44
74LS224	20.24
74LS240	0.42
74LS241	0.42
74LS242	0.42
74LS243	0.42
74LS244	0.42
74LS245	0.42
74LS247	0.44
74LS248	0.68
74LS249	0.99
74LS251	0.32
74LS253	0.44
74LS256	0.78
74LS257	0.34
74LS257A	0.46
74LS258	0.44
74LS258A	0.48
74LS259	0.48
74LS260	0.22
74LS266	0.32
74LS273	0.42
74LS275	POA
74LS279	0.33
74LS280	0.86
74LS283	0.45
74LS290	0.48
74LS292	16.86
74LS293	0.38
74LS294	17.82
74LS295	1.11
74LS295A	1.15
74LS298	0.98
74LS299	1.53
74LS321	3.82
74LS322	POA
74LS322A	POA
74LS323	3.24
74LS347	2.86
74LS348	1.98
74LS352	1.68
74LS353	1.68
74LS363	2.10
74LS364	POA
74LS365	0.30
74LS365A	0.34
74LS366	0.36
74LS366A	0.42
74LS367	0.29
74LS367A	0.34
74LS368	0.36
74LS368A	1.72
74LS373	0.38
74LS374	0.44
74LS375	0.42
74LS377	0.66
74LS378	0.98
74LS379	0.99
74LS381A	4.96
74LS385	3.48
74LS386	0.98
74LS390	0.46
74LS393	0.40
74LS395	0.66
74LS395A	0.94
74LS396	POA
74LS398	POA
74LS399	0.81
74LS423	0.98
74LS445	POA
74LS450	10.68
74LS461A	7.16
74LS465	3.82
74LS467	7.78
74LS468	7.78
74LS469	6.10
74LS469A	6.70
74LS490	2.85
74LS491A	12.82
74LS502	POA
74LS540	0.80
74LS541	0.80
74LS569	POA
74LS573	1.34
74LS574	1.34
74LS590	4.85
74LS592	5.28
74LS593	6.79
74LS595	4.85
74LS597	4.95
74LS621	POA
74LS622	POA
74LS623	2.98
74LS624	2.10
74LS625	5.37
74LS626	POA
74LS627	POA
74LS628	1.78
74LS629	1.98
74LS631	POA
74LS639	POA
74LS640	0.98
74LS641	0.98
74LS641-1	1.28
74LS642	0.98
74LS642-1	POA
74LS643	POA
74LS644	POA
74LS645	1.12
74LS645-1	1.28
74LS646	5.85
74LS652	POA
74LS669	1.07
74LS670	0.78
74LS673	POA
74LS674	17.60
74LS682	2.62
74LS683	POA
74LS684	3.85
74LS685	POA
74LS686	POA
74LS687	POA
74LS688	1.98
74LS693	POA
74LS794	POA
74LS795	POA
74LS796	POA
74LS797	POA
74LS848	POA

74HC SERIES

74HC00	0.19
74HC02	0.19
74HC03	0.24
74HC04	0.19
74HCU04	0.24
74HC05	0.20
74HC08	0.20
74HC10	0.29
74HC11	0.20
74HC14	0.25
74HC14A	0.34
74HC20	0.22
74HC21	0.22
74HC27	0.22
74HC30	0.22
74HC32	0.22
74HC42	0.48
74HC51	0.29
74HC58	0.42
74HC73	0.34
74HC74	0.25
74HC75	0.40
74HC76	0.40
74HC77	0.51
74HC85	0.48
74HC86	0.28
74HC93	0.44
74HC107	0.39
74HC109	0.35
74HC112	0.40
74HC113	0.40
74HC123	0.40
74HC125	0.40
74HC126	0.47
74HC131	0.52
74HC132	0.32
74HC133	0.32
74HC137	0.76
74HC138	0.34
74HC139	0.31
74HC141	0.61
74HC147	0.61
74HC148	0.55
74HC151	0.40
74HC153	0.40
74HC154	0.98
74HC155	0.69
74HC157	0.42
74HC158	0.47
74HC160	0.64
74HC161	0.42
74HC162	0.64
74HC163	0.42
74HC164	0.42
74HC165	0.55
74HC166	0.88
74HC173	0.76
74HC174	0.42
74HC175	0.36
74HC181	1.94
74HC182	0.59
74HC190	0.67
74HC191	0.52
74HC192	0.77
74HC193	0.54
74HC194	0.67
74HC195	0.47
74HC221	0.44
74HC237	0.73
74HC238	0.64
74HC240	0.44
74HC241	0.44
74HC242	0.80
74HC243	0.88
74HC244	0.43
74HC245	0.44
74HC251	0.35
74HC253	0.52
74HC257	0.47
74HC258	0.73
74HC259	0.65
74HC266	0.36
74HC273	0.54
74HC279	0.51
74HC280	0.89
74HC283	0.58
74HC298	0.73
74HC299	1.09
74HC323	1.58
74HC354	0.55
74HC356	0.65
74HC365	0.41
74HC366	0.52
74HC367	0.47
74HC368	0.52
74HC373	0.44
74HC374	0.44
74HC375	0.76
74HC377	0.51
74HC386	0.29
74HC390	0.38
74HC393	0.41
74HC423	0.64
74HC521	0.95
74HC533	0.95
74HC534	0.89
74HC540	0.69
74HC541	0.60
74HC563	0.88
74HC564	0.88
74HC573	0.64
74HC573A	0.72
74HC574	0.64
74HC589	1.64
74HC590	0.94
74HC592	1.19
74HC593	1.66
74HC595	0.92
74HC597	0.98
74HC620	1.62
74HC623	1.62
74HC633	1.62
74HC640	1.32
74HC643	1.32
74HC645	1.40
74HC646	1.77
74HC648	1.77
74HC651	1.47
74HC652	1.47
74HC658	4.49
74HC659	4.49
74HC664	4.49
74HC665	4.49
74HC670	1.10
74HC677	3.78
74HC678	5.91
74HC680	3.83
74HC682	4.21
74HC684	5.70
74HC688	0.87
74HC690	1.62
74HC691	1.62
74HC692	1.73
74HC693	1.73
74HC696	1.48
74HC697	1.24
74HC698	1.24
74HC699	1.24
74HC4002	0.35
74HC4015	1.07
74HC4016	0.44
74HC4017	0.42
74HC4020	0.52
74HC4022	0.56
74HC4024	0.50
74HC4028	0.58
74HC4040	0.50
74HC4046	1.54
74HC4049	0.48
74HC4050	0.36
74HC4051	0.64
74HC4052	0.68
74HC4053	0.68
74HC4053A	1.10
74HC4060	0.47
74HC4061	2.52
74HC4066	0.46
74HC4066A	0.54
74HC4067	4.72
74HC4072	0.45
74HC4075	0.32
74HC4078	0.46
74HC4094	0.64
74HC4316	0.68
74HC4351	0.89
74HC4511	0.55
74HC4514	1.38
74HC4515	1.42
74HC4518	0.80
74HC4520	0.72
74HC4534	0.00
74HC4538	0.68
74HC4543	0.81
74HC7001	1.01
74HC7002	1.01
74HC7032	1.01
74HC7266	0.84
74HC7074	1.99
74HC7292	1.10
74HC7294	1.10
74HC40102	1.10
74HC40103	1.10
74HC40105	1.40

74HCT SERIES

74HCT00	0.22
74HCT02	0.22
74HCT03	0.26
74HCT04	0.22
74HCT08	0.22
74HCT10	0.22
74HCT11	0.22
74HCT14	0.26
74HCT20	0.26
74HCT21	0.26
74HCT27	0.26
74HCT30	0.26
74HCT32	0.22
74HCT42	0.46
74HCT73	0.36
74HCT74	0.26
74HCT75	0.36
74HCT85	0.60
74HCT86	0.36
74HCT93	0.58
74HCT107	0.40
74HCT109	0.42
74HCT112	0.42
74HCT123	0.64
74HCT125	0.56
74HCT126	0.56
74HCT132	0.50
74HCT137	0.52
74HCT138	0.32
74HCT139	0.45
74HCT147	0.68
74HCT151	0.52
74HCT153	0.44
74HCT154	1.24
74HCT157	0.44
74HCT158	0.48
74HCT160	0.56
74HCT161	0.56
74HCT162	0.84
74HCT163	0.56
74HCT164	0.52
74HCT165	0.52
74HCT166	0.52
74HCT173	0.52
74HCT174	0.52
74HCT175	0.52
74HCT181	3.24
74HCT182	0.96
74HCT190	0.64
74HCT191	0.64
74HCT192	0.94
74HCT193	0.64
74HCT194	1.13
74HCT195	1.16
74HCT221	0.98
74HCT237	0.94
74HCT238	0.51
74HCT240	0.55
74HCT241	0.55
74HCT242	0.76
74HCT243	0.76
74HCT244	0.57
74HCT245	0.52
74HCT251	0.86
74HCT253	0.51
74HCT257	0.54
74HCT258	0.72
74HCT259	0.78
74HCT273	0.68
74HCT280	0.98
74HCT283	0.90
74HCT297	0.82
74HCT299	1.64
74HCT354	1.28
74HCT356	1.28
74HCT365	0.54
74HCT366	0.80
74HCT367	0.54
74HCT368	0.80
74HCT373	0.44
74HCT374	0.55
74HCT377	0.64
74HCT390	0.68
74HCT393	0.68
74HCT394	0.00
74HCT423	0.62
74HCT533	1.44
74HCT534	0.75
74HCT540	0.64
74HCT541	0.64
74HCT563	0.98
74HCT564	0.78
74HCT573	0.64
74HCT574	0.64
74HCT583	0.00
74HCT597	1.52
74HCT640	1.34
74HCT643	1.34
74HCT645	1.11
74HCT646	2.40
74HCT648	1.90
74HCT651	1.64
74HCT652	0.00
74HCT670	1.10
74HCT673	1.64
74HCT688	1.10
74HCT4002	0.39
74HCT4015	1.13
74HCT4016	0.52
74HCT4017	0.68
74HCT4020	0.74
74HCT4024	0.68
74HCT4040	0.70
74HCT4046	2.10
74HCT4051	0.96
74HCT4052	0.96
74HCT4053	0.84
74HCT4059	2.24
74HCT4060	0.84
74HCT4066	0.66
74HCT4067	4.93
74HCT4075	0.36
74HCT4094	0.84
74HCT4316	0.68
74HCT4351	1.04
74HCT4510	1.54
74HCT4511	0.94
74HCT4514	1.64
74HCT4515	2.50
74HCT4516	1.61
74HCT4520	0.90
74HCT4538	1.02
74HCT7007	0.39
74HCT7046	2.80
74HCT40102	2.43
74HCT40103	1.48
74HCT40104	2.71
74HCT40105	1.82

74HC SERIES SURFACE MOUNT

74HC00M	0.32
74HC02M	0.32
74HC03M	0.32
74HC04M	0.32
74HCU04	0.32
74HC08M	0.32
74HC10M	0.32
74HC14M	0.36
74HC20M	0.36
74HC30M	0.36
74HC32M	0.36
74HC74A	0.36
74HC75M	0.34
74HC85WM	0.65
74HC86M	0.36
74HC123AM	0.46
74HC125M	0.46
74HC132M	0.42
74HC138M	0.38
74HC139M	0.38
74HC154WM	0.64
74HC157M	0.38
74HC161M	0.48
74HC164M	0.48
74HC165M	0.57
74HC173M	0.48
74HC174M	0.38
74HC221AM	0.65
74HC240WM	0.55
74HC244WM	0.55
74HC245AW	0.62
74HC251M	0.42
74HC259M	0.69
74HC273WM	0.55
74HC367WM	0.53
74HC373WM	0.55
74HC374WM	0.55
74HC390M	0.57
74HC393M	0.53
74HC540WM	0.76
74HC541WM	0.76
74HC573WM	1.09
74HC574WM	0.84
74HC688WM	0.84
74HC4017M	0.48
74HC4020M	0.48
74HC4040M	0.44
74HC4046M	1.68
74HC4060M	0.48
74HC4066W	0.84
74HC4538M	0.78

74F SERIES

74F00	0.28
74F02	0.28
74F04	0.28
74F06	0.74
74F07	0.74
74F08	0.28
74F10	0.28
74F11	0.28
74F13	0.62
74F14	0.41
74F20	0.28
74F27	0.28
74F30	0.28
74F32	0.28
74F37	0.41
74F38	0.44
74F40	0.66
74F51	0.44
74F64	0.32
74F74	0.30
74F85	1.46
74F86	0.41
74F109	0.58
74F112	0.72
74F113	1.30
74F114	1.30
74F125	0.60
74F126	0.98
74F132	0.58
74F138	0.58
74F139	0.58
74F148	0.94
74F151	0.58
74F153	0.62
74F157	0.58
74F158	0.70
74F160	1.10
74F160A	1.10
74F161	1.10
74F162	1.28
74F163	1.28
74F164	1.28
74F166	4.32
74F168	4.48
74F169	3.60
74F174	0.76
74F175	0.76
74F181	4.48
74F182	1.80
74F189	4.98
74F190	3.40
74F191	3.20
74F192	3.20
74F193	3.20
74F194	1.48
74F195	2.24
74F219	4.38
74F224	POA
74F240	0.62
74F241	0.62
74F244	0.62
74F245	0.72
74F251	0.62
74F251A	0.66
74F253	0.62
74F257	0.62
74F257A	0.66
74F258	0.62
74F259	POA
74F260	0.78
74F269	7.48
74F273	0.84
74F280	0.68
74F283	0.92
74F299	POA
74F323	POA
74F350	1.50
74F352	0.64
74F353	1.14
74F365	1.28
74F366	1.30
74F367	1.48
74F368	1.30
74F373	0.62
74F374	0.62
74F377	0.92
74F378	1.56
74F381	3.68
74F385	POA
74F395	POA
74F399	0.98
74F412	POA
74F413	POA
74F432	POA
74F521	1.20
74F524	POA
74F533	1.20
74F534	1.20
74F537	1.60
74F538	1.60
74F539	1.60
74F540	1.98
74F541	1.98
74F543	3.98
74F544	POA
74F545	POA
74F547	POA
74F573	2.92
74F574	2.92
74F579	7.98
74F604	4.84
74F620	POA
74F621	POA
74F623	POA
74F646	5.15
74F676	POA
74F821	3.98
74F823	POA
74F825	POA
74F827	4.48
74F841	4.48
74F843	4.93
74F845	POA
74F1244	3.75

74AC SERIES

74AC00	0.38
74AC02	0.49
74AC04	0.40
74AC08	0.40
74AC10	0.40
74AC11	0.40
74AC14	0.40
74AC20	0.40
74AC32	0.40
74AC74	0.48
74AC109	0.64
74AC112	0.81
74AC138	0.65
74AC139	0.65
74AC151	0.68
74AC153	0.65
74AC157	0.81
74AC158	0.65
74AC163	0.80
74AC169	1.98
74AC174	0.65
74AC175	0.80
74AC191	1.38
74AC240	0.92
74AC241	0.92
74AC244	0.92
74AC245	1.10
74AC251	0.60
74AC253	0.60
74AC258	0.60
74AC273	1.10
74AC283	1.40
74AC299	2.06
74AC373	0.94
74AC374	0.92
74AC377	0.98
74AC540	0.98
74AC541	0.98
74AC573	1.38
74AC574	1.38
74AC646	POA
74AC648	POA

74C SERIES

74C00	0.56
74C02	0.56
74C08	0.56
74C10	0.56
74C14	0.56
74C20	0.98
74C30	0.98
74C32	0.68
74C42	2.88
74C48	2.98
74C73	1.28
74C74	0.94
74C76	1.26
74C85	1.86
74C90	1.29
74C93	2.10
74C95	1.60
74C150	5.40
74C151	3.94
74C154	5.82
74C157	3.80
74C164	2.54
74C165	2.54
74C221	2.98
74C240	2.08
74C244	2.08
74C373	2.08
74C374	2.08
74C901	1.18
74C902	1.18
74C903	1.52
74C906	1.10
74C907	1.10
74C908	2.20
74C911	14.42
74C912	14.42
74C914	1.16
74C915	2.74
74C922	6.80
74C923	6.80
74C925	9.30
74C926	9.30
74C929	9.30

74S SERIES

74S00	0.44
74S02	0.44
74S03	0.51
74S04	0.42
74S08	0.42
74S09	0.48
74S10	0.98
74S11	0.48
74S20	0.48
74S32	0.78
74S40	0.25
74S51	0.36
74S64	0.36
74S74	0.98
74S86	1.12
74S112	1.08
74S124	2.42
74S132	0.98
74S133	0.73
74S134	1.95
74S138	0.88
74S139	0.88
74S140	0.78
74S153	1.26
74S157	1.72
74S163	2.60
74S174	0.92
74S175	1.35
74S182	3.29
74S189	2.14
74S195	2.40
74S240	1.00
74S241	1.12
74S244	1.77
74S257	1.22
74S258	1.22
74S260	0.70
74S273	2.44
74S274	2.42
74S280	0.96
74S283	1.90
74S374	2.18
74S394	2.10
74S412	2.10
74S436	2.62
74S437	2.62
74S472	2.32
74S734	2.62

VOLTAGE REGULATORS

78008AP	1.15
7805	0.28
7805A	0.32
7805FA	0.45
7806	0.28
7808	0.28
7809	0.32
7812	0.28
7812A	0.32
7812CTC	0.32
7815	0.28
7818	0.28
7824	0.28
78L05	0.24
78L05A	0.28
78L05ACLP	0.40
78L05ACZ	0.28
78L12	0.28
78L12A	0.28
78L12ACZ	0.30
78L15	0.28
78L24	0.28
78L56	1.10
78M05	0.32
78M05A	0.36
78M12	0.32
78M12A	0.36
78M13A	0.65
78M15	0.32
78S05	0.48
78S12	0.48
78S15	0.55
7905	0.28
7905A	0.32
7905FA	0.60
7909	0.55
7912	0.30
7912A	0.36
7912FA	0.78
7915	0.30
7918	0.30
7924	0.30
79L12A	0.35
79L12ACP	0.35
79M05	0.42
79M05A	0.42
79M05FA	0.65
79M12	0.50
79M12A	0.60
LM317T	0.50
LM317MP	1.06
LM317LZ	0.55
LM338K	4.45
UA78GU1C	1.02
UA79GU1C	1.02
RC4195N	1.80

DIODES

1N2986RB	18.20
1N3881	2.54
1N3997A	6.55
1N4001	0.04
1N4002	0.04
1N4003	0.04
1N4006	0.04
1N4007	0.04
1N4148	0.03
1N4149	0.06
1N4150	0.08
1N4446	0.06
1N4728A	0.24
1N4735A	0.24
1N4736A	0.24
1N4740A	0.24
1N4743A	0.24
1N4744A	0.24
1N4756A	0.24
1N5226B	0.09
1N5232B	0.09
1N5234B	0.09
1N5337B	0.48
1N5349B	0.48
1N5352B	0.48
1N5357B	0.48
1N5365B	0.48
1N5366B	0.48
1N5370B	0.48
1N5380B	0.48
1N5401	0.11
1N5402	0.11
1N6287A	1.55
1N825	1.80
1N825A	1.34
1N827	1.40
1SS252	0.20
5082-2800	0.66
5082-2810	1.40
5082-2835	0.44
AA119	0.60
AA144	0.72
AAZ15	0.58
AAZ17	0.58
AAZ18	0.48
BAV10	0.08
BAV45	4.98
BAW62	0.06
BAX16	0.06
BB204	0.32
BB212	2.48
BB405B	0.22
BB809	0.60
BY179	0.42
BY260-200	3.58
BY261-200	3.98
BYV28-100	0.99
BYV32-50	1.60
CV8805	0.60
DS16C	0.40
MV1404	15.90
MV209	1.20
OA200	0.10
OA202	0.20
OA47	0.14
OA90	0.14
P6KE36A	0.88
P6KE47A	0.88
REC53A	0.40
ZPD2.7V	0.06

ZENER DIODES MISC.

BZY93C7V5	2.66
BZY93C15	2.66
BZY93C18R	2.66
BZY93C20	2.66
BZY93C24V	2.66
BZY93C33R	2.66
BZT03C120	0.40
BZX61C9V2	0.09
BZX61C24V	0.09

ZENER DIODES 400mW
2.4V to 75V
Price: 6p each

ZENER DIODES 500mW
2.4V to 200V
Price: 6p each

ZENER DIODES 1.3 WATT
2.7V to 200V
Price:10p each

ZENER DIODES 3.0 WATT
7.5V to 270V
Price:40p each

ZENER DIODES 5.0 WATT
3.3V to 200V
Price:42p each

ZENER DIODES STUD MOUNT 20 WATT
7.5V to 75V
Price: £4.94 ea.

BRIDGE RECTIFIERS

0.9A/200VDIL	0.38
3.0A/200V SIL	0.57
6A/100V SIL	1.60
8A/200V SIL	1.96
35A/100V Sqr	2.98
KBPC1002	1.64
KBPC3502	2.98
W005- 1A/50V	0.32
W02G- 1.5A	0.40
2W02	0.40
2KBB10R/SIL	0.66
2KBB20R/SIL	0.70
B80C1500/Sq	0.35
B80C1500SIL	0.60
SKB6008/60A	POA

CRYSTALS

HC49(HC18/U)

Freq.MHz	
1.843200	1.60
2.000000	1.66
2.457600	1.49
3.276800	0.98
3.579545	1.10
3.686400	1.02
4.000000	1.02
4.096000	1.10
4.194304	1.10
4.433619	1.10
4.608000	1.10
4.915200	1.20
5.000000/S	1.02
5.068800	1.10
5.242880	1.20
5.888200	1.80
6.000000	1.02
6.144000	1.02
6.400000	1.64
6.552000	1.40
6.553600	1.21
7.372800	0.78
8.000000	1.00
8.867230	1.34
9.830400	1.20
10.00000	1.10
10.69500	1.90
11.00000	1.10
12.00000	0.92
13.87500	2.40
14.00000	1.64
14.31818/S	0.85
14.74560/S	1.10
14.74560	1.10
15.00000/S	1.10
16.00000	1.02
16.00000/S	1.20
18.43200/S	1.10
19.66080/S	1.20
20.00000/S	1.60
22.11840/S	1.68
24.00000/S	1.82
27.64800/S	1.20
30.00000/S	6.99
32.00000/S	1.40
48.00000/S	1.68

S = Series

HC33/U

0.204800	8.23
0.307200	6.99
1.000000	3.95
1.843200	3.71
2.000000	4.65
2.097152	3.71
2.457600	1.92
2.500000	1.92
3.000000	2.25

HC49/U4H

3.276800	1.66
3.579545	1.58
5.068800	2.25
7.864320	1.49
8.000000	1.14
10.00000	2.25
11.05920	2.40
12.00000	1.14
14.00000	2.25
16.00000	1.14
20.00000	1.52
24.00000	1.90

UM-1

8.000000	2.25
8.192000	2.02
10.00000	2.25
11.00000	2.25
12.28800	2.66
15.00000	2.25
17.73447	2.80
18.00000	2.50
20.00000	2.25
21.00000	2.25
24.00000	2.80

CRYSTALS MISC.

HC43/T	
1.000000	6.99
MINI CYLINDER	
0.032768	0.88
WATCH	
0.032768	0.82

CRYSTAL OSC. MODULES

8pin DIL Plastic pkg TTL Output
4 Pins spaced at corners of 8pinDIL

Freq.= MHz
4, 4.9152, 8, 10, 12, 16 & 20
Price: £2.98 ea.

24, 32, 40 & 50MHz
Price £3.40 ea.

8pin DIL Sealed Metal Package HCMOS Output

13.2mm sq.
Pins spaced at corners of 8pinDIL
Freq.= MHz
3.6864,4,8,10,12,16, 20,24,32,40 & 50
Price: £4.20 each

TTL Output 14pin DIL Layout Sealed Metal 4pin Pkg
Freq.= MHz
1MHz **£8.90 ea.**

4,4.9152,6,8,9.8304, 10,12,15,16. 18.432, 19.6608, 20, 24, 25 & 30MHz
Price: £3.52 ea.

30, 32, 32.768, 33.33, 40 & 50MHz
Price: £4.45 ea.

Programmable Crystal Oscillators

EXO-3C SERIES 8pin DIL Plastic Package
Freq.= MHz
12, 14.31818, 16, 16.384,19.6608 & 20MHz
Price: £3.92 ea.

16pin DIL Plastic Package
Programmable for 57 Diff.Frequency

SPG8640AN
0.005 to 600kHz

SPG8640BN
0.0083 to 1MHz

SPG8640CN
0.064 to 768kHz

SPG8650BN
0.00083 to 100kHz

Price: £ 9.25 ea.

DC to DC Converters

TDK CE-0344	5.60
3W5R 15-15	27.50
IPL S.010	23.40

1 Watt DC/DC 5V input ±Output DIL & SIL by Newport
NMA0505±5V
NMA0509±9V
NMA0512±12V
NMA0515±15V
Price:£7.90ea.

DC/DC Converters by Computer Products

PM623	24.60
PM671	26.70
PM672	26.70
PM903	44.00
PM951	46.50

RESISTORS

METAL FILM 0.25W 1%
E24 Series
10R to 1M 3p each
N.B. Min Qty. Order
Min. 5pcs per value

METAL FILM PRECISION 0.25 WATT 0.1%
E96 Series
100R to 255K
Price: £0.94 each

HIGH PRECISION NON-INDUCTIVE WIRE WOUND 0.15 WATT 0.1%

Temp.Coeff.3ppm
10R,50R,100R,250R, 10K,100K
Price: £3.85 each

HIGH PRECISION NON-INDUCTIVE WIRE WOUND 0.33 WATT 0.1%

Temp.Coeff.3ppm
1R,5R,10R,20R,50R
Price: £3.60 each

100R,120R, 250R, 500R,1K, 2K, 5K, 10K,20K
Price: £3.10 each

MEMORIES

DYNAMIC RAM

4164-10	1.40
4164-12	1.20
4164-15	1.20
41256-8	2.40
41256-10	2.40
41256-12	2.40
41264-15	2.24
41464-12	4.45
41464-10	4.45
4464-10	2.80
414256A-70	3.90
44C256AZ-10	6.95
44C256-8	5.00
511000-85	8.45
HM48416AP-15	4.60
HM48416AP-20	4.25
HY53C256LS-80	1.60
HY53C464LS-80	3.95
HYB511000-85	8.45
KM44C256AZ-10	6.95
M5M4464P-15	4.60
MK4116N-54	2.80
MK4564N-15	1.20
NMC3764N-15	1.60
UPD41464C-12	4.20
UPD41464C-15	4.20
UPD416C-2	3.40
UPD416C-3	3.65
UPD446D-1	2.60

STATIC RAM

2114-3L	3.40
6264LP-10	2.40
6264LP-12	2.40
62256LP-12	4.95
62256LP-10	4.95
CDM6116AE3	5.30
CDM6117AE3	5.85
HM1-6116-5	4.38
HM3-6116-5	3.60
HM6116LP-2	2.60
HM6116LP-3	2.60
HM6117LP-3	5.75
HM62256LP-10	7.93
HM6264ALP-12	3.95
HM6264ASP-20	3.95
HM6267P-35	5.07
HM628128LP-80	18.55
HM66204L-12	15.80
KM62256ALP-10	4.95
LH5164D-10L	2.40
P2114AL-2	3.40
P2114AL-4	3.40
PCD5101P	3.30
UPD43256AGU10L	8.33
UPD43256C-12	5.60
UPD4364C-15	4.70

UVPROMS

27C128-25	3.95
27C64A-15	3.95
27C256-15	3.95
27C256-25	3.95
D27256	5.40
27C512D-12	6.48
27C1000D-12	8.92
27C4096-12	POA
HM27C101G-20	9.80
HN27C1024HG10	16.63
HN27C64FP-20T	3.40
HN27C64G-15	4.20
HN27C64G-20	4.20
HN462532P	4.50
HN4827128G-25	4.55
HN482764G	3.80
M2716-1F1	3.50
M5L2732K	4.40
M5L2764K	3.30
MBM27C64-20/21V	4.90
MBM27C128-30	4.20
MBM27C256-30	5.10
NMC27C256Q-25	4.95
NMC27C64Q-25	3.66
TMS2516JL-45	4.58
TMS27128JL-25	4.60
TMS2716JL-45	4.60
UPD27256D/21V	5.60
UPD2732A/21V	4.95
UPD27C256D-15	5.80
UPD27C512D-15	6.96
UPD27C64D-25	4.95

EEPROMS

28C64-25	9.80
28C64-15	10.95
28C256-20	25.84
28C256-15	27.50
28C256-15DC	28.50
X2816AD	5.10
X2816AP-25	5.10
X2864AP-35	12.20
24C01	1.62
24C02	2.10
24C04	2.98
24C16	5.40
28C04A-20	4.40
59C11	1.44
93C06	1.12
93C46	1.28

MISC. MEMORIES

6341-1J	4.58
AM2148-45DC	5.44
AM27S281PC	3.98
IDT7130LA-100P	POA
IDT7132LA-100P	POA
MB8414E	4.95
MCM4027AC3	2.80
N82S126AN	2.49
N82S153N	5.80
N82S181AN	6.09
NMC6504J-9	3.40
NMC9306N	1.45
P5101L-1	3.90
TBP18S030N	1.74
TBP24S10N	2.90
TBP24SA10N	3.15
TC5501P	3.50
TC5504AP-2	3.40
TC5516PL-15	4.20
TC5517AP-2	4.20
TC5565PL-15	3.60
TMS4014JDL	3.40

CAPACITORS SURFACE MOUNT

Multilayer Ceramic
63 VOLT
Case Size: 1206
L2xW1.25mm

10pF 22pF 33pF 47pF
100pF 220pF 330pF
470pF 1000pF 2200pf
3300pF 4700pF 10000, 22000pF 33000pF
Price: 15p each

47000pF 100000pF
Price: 18p each

MICROPROCESSOR & SUPPORT ICs

100114DEC	7.40
100141DC	9.80
6303XP	8.76
6321P	4.20
63485CP32/sm	19.95
63B03XP	10.07
6502	3.98
6502A	5.40
6520P	4.40
6522	4.40
6522A	5.26
6551	4.43
6551A	4.43
65C02P2	5.84
65C02P3	6.98
65C102P2	7.00
65C22P2	4.80
65C51E-1	3.80
65C51E-2	4.38
68000P-10	6.98
68000P-16	18.20
68000P-8	6.50
68008P-8	7.85
68010P-12	POA
6802P	3.40
6803AP	POA
6805E3E	10.98
6810P	POA
6821P	1.52
6840P	3.40
6844P	17.20
6845P	4.86
6845SP	5.40
68A00P	POA
68A09P	4.30
68A21P	1.98
68A40P	2.56
68A50P	2.98
68B09P	3.98
68B21P	1.98
68B40P	2.98
8080A	4.96
8085AH-2	5.98
8086	3.40
8086-2	3.90
80C286-12/pga	48.50
80C286-8/plcc	24.40
80C85A	4.95
80C85A-2	5.94
8118-5CH	7.60
93L34DC	7.08
AM25LS2568P	2.68
AM25LS2569P	2.68
AM2602PC	2.30
AM26LS31DC	2.30
AM26LS31PC	1.26
AM27S191ADC	10.20
AM27S281PC	6.25
AM2964BDC	12.36
AM2965DC	6.36
AM2966PC	3.98
AM29826DC	3.34
AM685DL	9.82
AM8238PC	5.60
AM9050CDC	4.95
AM9050CPC	4.60
AM9102CPC	2.82
AM9114BDM	9.96
AM9551PC	9.66
AM96L02PC	3.35
AY-5-8136	6.45
AY-5-8136-006	6.45
C1164/SMD	4.98
C8231A	59.00
C8253	3.60
CA80C85B	5.98
CD82C85	9.62
CD82C86H-5	9.74
CG80C286-12	48.50
CG80C286-16	65.00
COM8136	6.45
COM81C17	8.15
CP82C54	6.42
CRT-8004-001	9.65
CS8205	8.92
D3232	5.60
D8086	5.48
D8086-2	8.80
D8202A	POA
D8254-2	6.42
D8284A	3.90
D8288	6.48
D82C284-12	9.60
D82C284-8	7.85
D82C288-10	10.96
D82C288-12	11.85
D82C288-8	9.36
D8748H	9.95
DM9601N	2.45
DP8228N	6.36
DP8238N	6.36
DP8304BN	2.34
DP8311N	6.54
DS1221	6.44
DS1231-20	4.44
DS1232	3.26
DS3486N	3.20
DS3487N	3.20
DS34C86N	4.80
DS34C87N	4.80
DS3631N	3.33
DS3632N	2.81
DS3633N	3.33
DS3634N	2.81
DS3691N	4.96
DS3862N	7.38
DS5000-32-12	47.50
DS8640N	1.20
DS8820AN	2.95
DS8832N	2.68
DS8836N	2.44
DS8837N	2.40
DS8838N	2.40
EF6803A-1P	3.80
EF6803P	3.80
EF6821P	1.30
EF68B09P	3.18
EF68B21P	1.44
EP610PC-35	POA
HD1-0165-5	10.96
HD146818AP	4.20
HD3-6402-9	6.16
HD3-6440-9	8.89
HD3-6495-9	8.89
HD44883	9.52
HD46505SP	9.85
HD46802P	5.50
HD6321P	4.20
HD63485PS32	32.50
HD63B03XP	11.95
HD68000-8	11.59
HD6845SP	6.92
HD68A52P	5.60
HD68B21P	4.29
HI3-7159-5	20.98
HI3-7159A-5	23.40
HM10422	14.30
ID82C86H	17.06
IM6402AIPL	10.20
IM6402IPL	7.75
IM6403IPL	10.80
IMS2600P-15	4.40
INS8250N	7.80
INS8250N-B	7.80
M5M82C51AP	4.20
M5M82C54P-6	5.40
MAB8031AH12P	4.56
MAB8035HL-6P	5.98
MC10103P	1.98
MC10115L	3.21
MC10115P	1.98
MC146805E2P	9.18
MC68000P12/16	POA
MC68010P10/12	POA
MC6802P	2.47
MC6809P	6.78
MC6821P	1.80
MC6840P	5.05
MC6844P	18.40
MC6845P	7.38
MC6850P	3.35
MC68705R3P	25.35
MC68A00P	7.02
MC68A09P	7.62
MC8314P	6.60
MCM6810P	3.00
MCM68A10P	5.35
MM53200N	3.40
MM58167BN	10.64
MM58174AN	14.80
MM58274CN	9.18
MSM5832RS	3.39
MSM80C35RS	4.90
MSM80C39/SMD	6.45
MSM80C85A	3.95
MSM80C85A-2	5.98
MSM80C86	7.60
MSM81C55	4.60
MSM82C51A	3.58
MSM82C53-2	3.98
MSM82C53-5	3.58
MSM82C54-2	4.20
MSM82C59A-2	3.98
MSM82C84A	3.30
MSM82C84A-2	3.60
MSM82C88	12.60
N80C286-10/pl	24.50
N80C286-12/pl	29.54
N80L286-8C2/pl	36.20
N8235N	3.68
N8264N	3.68
N82S126AN	3.25
N82S181F	10.04
NS16450N	4.68
NS16550AFN	12.60
NSC800N-1	10.80
P8032AH	4.29
P8051AH	11.20
P8052AH/Basic	23.45
P8080A	3.90
P8085A-2	5.98
P8085AH-2	5.98
P8088	4.80
P80C31BH	4.54
P80C86AL-2	12.60
P8155H/2	6.98
P8185	18.10
P8205	2.00
P8212	2.40
P8226	2.40
P8251A	3.90
P8253	2.80
P8255A-5	3.90
P8259	2.85
P8259A	3.20
P8274	9.98
P8279-5	3.20
P8282	2.64
P8286	3.60
P82C54	4.10
P82C54-2	4.80
PAL10L8CN	1.90
PAL12H6CN	1.90
PAL16R4BCN	2.17
PAL20L10CNS	4.35
PAL20X8CNS	3.32
PALC16L8Q-25CQ	6.10
PALC20L8Z-45CQS	5.17
PALC22V10H-35QS	8.34
PCD8584P	8.28
PCF8566P	8.28
PCF8566T	8.28
PCF8570P	7.85
PCF8573P	6.72
PCF8574P	5.90
PCF8574T	5.90
PCF8591P	9.35
R6502AP	5.70
R6520P	4.40
R6522	4.40
R6522AP	5.80
R65C02P2	5.84
R65C02P3	6.90
R65C02P4	8.95
R65C102P2	6.85
R65C21P2	5.94
R65C22P2	4.80
SAB80C32P	5.95
SAB8155-P	3.82
SAB8259AP	3.59
SAB82C54-2-P	4.12
SAB82C55A-2-P	4.80
SC80C451ccn64	13.60
SCN2661bc1n28	3.35
SCN2661ccn28	3.35
PAL16R4-15CN	2.98
TL16C552FN	12.58
TMP7002NL-2	4.97
TMP8085AP-2	5.98
TMS3477NL	6.68
TMS3700NSB	8.78
TMS3702ANS	8.78
TMS3835ANS	7.55
TMS77C01NL	10.74
TMS9900NL	24.40
TMS9901NL	14.16
TMS9902ANL	15.94
TMS9914ANL	23.10
TMS9928ANL	7.40
TMS9995JDL	69.85
UA9636ACP	1.98
UA9637A	1.98
UA9638CP	1.98
UA9639CP	1.98
UM6845B	4.95
UM9151	POA
UM9151-3	POA
UPB8238	POA
UPB8282C	4.98
UPB8284AD	4.98
UPB8286C	4.98
UPD70108C-10	9.10
UPD70108C-8	6.95
UPD70116C-10	12.90
UPD70116C-8	9.20
UPD71055C	4.38
UPD7201AC	11.68
UPD7201C	6.80
UPD765AC	5.42
UPD765AC	5.42
UPD780C-1	4.76
UPD80C39HC	8.42
UPD8155HD	5.84
UPD8251AFC	4.08
UPD8253C-2	3.32
UPD8253C-5	3.32
UPD8286C	POA
UPD8741AD	12.52
UPD8749HC	13.98
V20-10MHz	9.10
V20-8MHz	6.95
V30-10MHz	12.90
V30-8MHz	9.20
V61C30P	7.80
VC0106N6	8.60
Z0800110PSC	16.90
Z0868112PSC	3.20
Z180-MPU	POA
Z8001B-CPU	11.96
Z8018008VSC	8.25
Z80A-CPU	1.25
Z80A-CTC	1.98
Z80A-DART	3.15
Z80A-DMA	3.95
Z80A-PIO	1.25
Z80A-SIO/0	3.40
Z80B-CPU	1.52
Z80B-CTC	3.00
Z80B-DART	5.80
Z80B-DMA	POA
Z80B-PIO	2.20
Z80B-SIO	4.50
Z80C00AB6	2.98

TELECOM & SPECIAL FUNCTION ICs

62X0890-U18	3.70
707W02020	5.25
733W00124	5.25
AMA1503GXB	4.68
BAA1505	1.80
CLA25106/PLCC	5.95
GA05001GDB	3.20
KS-49258/PLCC	5.92
MJ1454BB	7.65
MK5175N	3.80
OC-147-7	2.40
PBD352303	4.35
PP34C108	6.80
Q4704	3.60
QMV16BP5	7.98
QMV18C	6.95
QMV18CN1	7.85
QMV18CW1	7.85
QMV25C	8.42
QMV62AW1	6.90
S4534-AMI	4.20
SA336931	2.95
SAA5025D	5.40
SCM66115P	3.40
SGS7P050	4.55
SP1450B	5.76
ULA1RB029E1	6.80
ULA20RK008E1	59.72
XR-T5683	3.60
ZNA2L029J-BS	3.80
ZNPCM1J-BS	8.95

OPTO ELECTRONICS

4N25	0.60
4N26	0.60
4N33	0.40
4N38	0.56
6N139	1.60
CNX36	0.38
CNY17-3	0.64
CNY21N	POA
DF08	0.40
HCPL-2200	5.98
HCPL-2231	5.98
HCPL-2602	5.68
HCPL-2630	3.68
HCPL-2730	3.45
HCPL-2731	3.20
HCPL-4200	5.98
ILD74	1.44
ILQ1	1.60
ILQ74	2.25
ISQ74	2.25
TIL100	1.98
TIL111	0.60
TIL113	0.60
TIL117	0.85
TIL119	1.20
TIL311	9.65
TLP504A	1.58
TLP521-4GB	4.20
TORX173	4.96
TOTX173	4.96

LINEAR & MISCS.

3630BM/BB	3.40
49620/BB	POA
555-TIMER	0.20
6341-1J	POA
741-OPAMP	0.18
AD0P07CN	2.14
AD520JN	POA
AD524	21.52
AD534JH	POA
AD537JH	POA
AD548JN	1.80
AD578JN	POA
AD581JH	8.92
AD581KCSA/SMD	9.97
AD585AQ	POA
AD592CN	POA
AD594AD	12.64
AD595AD	10.20
AD648JN	3.40
AD707JN	3.40
AD711JN	2.34
AD712JN	3.72
AD7245JN/KN	POA
AD741KN	3.69
AD7523KN	9.80
AD7537JN	32.98
AD7537LN	POA
AD7542KN	POA
AD7543JCWE	POA
AD7578KN	46.15
AD844AN	8.75
ADC0804LCN	4.20
ADC0820CCN	22.40
ADC0834CCN	10.80
ADC804LCWM	12.10
ADC84KG-10	12.66
ADC908HP	18.42
ADDAC80N	POA
ADG201AKN	4.86
ADOP07CN	2.32
AH0015CD	17.20
AY-3-1270	3.60
AY-5-1013	3.20
AY-5-1013A	5.24
AY-3-1015D	3.60
AY-5-1250	POA
AY-5-3600-PRO	9.96
BA6109	1.68
BA6208	1.40
CA3046	0.51
CA3046(SMD)	0.89
CA3054	0.94
CA3059	1.20
CA3078AT	2.42
CA3079	0.88
CA3080E	0.70
CA3081	0.96
CA3089E	1.22
CA3094AE	2.16
CA3096AE	3.48
CA3096CE	1.82
CA3097E	2.60
CA3120E	POA
CA3130BT	19.20
CA3130E	1.10
CA3140AE	1.34
CA3140E	0.44
CA3146E	0.90
CA3160E	1.25
CA3240E	0.98
CA3240E1	2.16
CA324E	0.98
CA3260E	1.68
CA3280AE	5.94
CA3280E	3.42
CA555CE	0.20
CA741CE	0.18
CS5503-KD	POA
CX7925B	POA
D169CJ	POA
DAC0800LCN	4.10
DAC0832LCN	10.67
DAC08CP	2.60
DAC08EP	3.64
DAC1008LCN	10.73
DAC1222LCN	20.40
DG201ABK	3.83
DG211	1.56
DG508ACJ	3.98
DG508CJ	3.25
DS1488N	0.36
DS14C88M/SMD	1.65
DS14C88N	1.65
DS14C89AN	1.65
HA12017	1.44
HA13426	11.96
HA17723	1.10
HD75189P	POA
HEF4754V	22.20
HI1-0201-5	3.60
HI1-508A-5	11.21
HI1-549-5	POA
HI1-574AKD-5	42.50
HI3-0201-5	3.20
HI3-0509A-5	7.15
HI3-201-5	3.20
HIIL1	POA
HS574-AK	18.20
ICL7104-16CPL	26.08
ICL7107CQH/PLCC	5.20
ICL7109CPL	9.85
ICL7116CPL	6.74
ICL7117CPL	6.74
ICL7126CPL	6.74
ICL7135CPI	8.98
ICL7136CPL	6.94
ICL7137CPL	6.94
ICL7606CJN	12.24
ICL7611DCPA	1.32
ICL7621DCPA	1.98
ICL7622	POA
ICL7650CPD	4.98
ICL7650SCPD	6.27
ICL7652BCPD	8.24
ICL7652CPD	8.24
ICL7660CPA	1.40
ICL7660SCPA	3.80
ICL7662CPA	4.40
ICL7663BCJA	6.78
ICL7663BCPA	5.10
ICL7664CPA	7.95
ICL7665ACPA	4.98
ICL7673CPA	1.38
ICL8052ACPD	8.73
ICL8068AJD	11.38
ICL8069CCSQ	3.75
ICL8069DCSQ	2.88
ICL8069DCZR	2.88
ICL8211CPA	2.56
ICL8212CPA	2.48
ICM7170IPG	6.42
ICM7207AIPD	6.42
ICM7207IPD	6.42
ICM7209IPA	3.75
ICM7211AMIPL	4.68
ICM7211MIPL	4.68
ICM7212AMIPL	3.88
ICM7213IPD	4.58
ICM7216AIJI	22.44
ICM7217AIPI	9.20
ICM7217BIJI	10.42
ICM7217IJI	10.42
ICM7218AIJI	6.85
ICM7218AIPI	6.85
ICM7218DIJI	6.85
ICM7218EIJL	14.76
ICM7224IPL	8.98
ICM7226AIJL	26.12
ICM7226BIPL	23.54
ICM7249IDM	POA
ICM7555IBA	2.40
ICM7555IPA	0.84
ICM7556IPD	1.85
IM6403IPL	10.80
L272	2.10
L272M	2.10
L293E	3.90
L297A	4.69
L4805CV	2.20
L487	3.15
L4960	3.15
L702B	2.94
LA6250	POA
LA6358	POA
LA6510	POA
LA6520	POA
LC7132	POA
LC7522	POA
LC7555	POA
LD111ACJ	POA
LF13508D	18.20
LF311H	10.80
LF347N	2.40
LF351N	0.98
LF353N	0.86
LF355N	1.82
LF356N	1.82
LF357BN	4.98
LF357M/SMD	4.98
LF357N	1.20
LF398N	3.98
LF411CN	1.48
LF412CN	1.98
LF441CN	0.75
LF442CN	0.99
LF444CN	2.71
LH0002CN	10.80
LH0032CG	33.60
LM101AH	5.65
LM10CN	9.24
LM111H	6.74
LM13600N	3.40
LM13700N	3.40
LM1391N	3.40
LM139J	6.60
LM1458N	0.82
LM1496N	2.95
LM1801N	7.92
LM1881N	4.80
LM1889N	7.40
LM1894N	4.16
LM218H	15.75
LM239N	3.90
LM2901N	1.25
LM2903N	1.25
LM2904N	1.25
LM2917N-14	6.10
LM2917N-8	5.80
LM294OCT15	2.95
LM294OCT5	2.50
LM2984CT	7.50
LM301AN	0.36
LM307N	1.39
LM308N	1.65
LM310N	2.98
LM311N	0.64
LM311N-14	2.15
LM312H	8.95
LM317AT	2.60
LM317T	0.52
LM317T-SGS	0.52
LM318N	2.98
LM319N	2.84
LM320LZ-12	0.34
LM324AN	3.66
LM324J	2.47
LM324N	0.64
LM325N	9.40
LM3301N	2.60
LM334Z	2.20
LM335Z	2.48
LM336Z-2.5	1.48
LM336Z-5.0	1.48
LM337T	1.15
LM339AN	2.98
LM339N	0.60
LM340AT12	1.98
LM340T-5	0.48
LM340T12	0.48
LM340T15	0.30
LM340T5	0.30
LM343H	8.80
LM346N	3.96
LM348DP	0.40
LM348N	0.40
LM350T	6.85
LM351N	2.60
LM358N	0.32
LM359N	4.68
LM360H	7.72
LM361M/SMD	6.40
LM363H-100	16.50
LM369DN	3.82
LM369DRC	3.70
LM380N	1.20
LM381AN	7.88
LM385Z-1.2	2.20
LM385Z-2.5	2.20
LM386M-1/SMD	1.65
LM386N-1	1.40
LM386N-3	1.80
LM386N-4	2.60
LM387AN	5.90
LM388N-1	4.25
LM389N	3.40
LM3900N	1.60
LM3909N	2.64
LM3914N	4.40
LM393N	0.30
LM393P	0.30
LM394CN	5.98
LM3999Z	2.76
LM399H	7.85
LM4250J	11.82
LM555CN	0.28
LM565CN	7.48
LM710CH	2.80
LM723CH	2.80
LM723CN	0.70
LM733CN	2.65
LM741CJ-14	2.20
LM741CN	0.45
LM747CH	2.40
LM747CN	0.90
LM78GCP	2.40
LM79GCP	2.40
LM833N	2.82
LS285AB	2.40
LS288B	3.60
LS7210	4.40
LT1006CNB	2.72
LT1010CT	4.58
LT1028CN8	7.32
LT1032CN	4.70
LT1070CT	9.14
LT1083CP	8.82
LT1086CT	2.90
LTC1052	7.97
LTC485CN8	2.16
LTC490	4.40
M5218AL	POA
M5220	POA
M5238L	POA
M5298P	POA
M706B1	1.25
MAX1232CNG	POA
MAX1232CPA	3.57
MAX1259CPE	POA
MAX162ACNG	POA
MAX232ACPE	4.84
MAX232CPE	2.80
MAX232EWE	3.80
MAX232N	2.80
MAX280CPA	6.94
MAX452CPA	5.38
MAX627CPA	2.98
MAX660CPA	5.72
MAX690ACPA	6.58
MAX694CPA	POA
MAX697CPE	POA
MAX7219CNG	7.15
MAX8211CPA	2.28
MAX901BCPE	POA
MC1377P	4.93
MC1413P	0.74
MC14411P	11.38
MC14416L	17.60
MC14495P	4.82
MC145406P	2.10
MC1455P	0.40
MC1455P1	0.60
MC1458P	0.32
MC1488L	2.40
MC1488P	0.38
MC1489A	0.80
MC1489AL	2.25
MC1489AN	0.80
MC1489L	2.20
MC1489P	0.38
MC1496N	2.20
MC1558L	3.32
MC1648P	12.40
MC1658P	12.78
MC1709CPI	1.20
MC1723CP	1.20
MC1741CP	0.45
MC3242AP	7.54
MC3301P	0.88
MC3302P	0.60
MC3340P	1.60
MC3357P	3.20
MC3403P	1.40
MC3446AP	6.75
MC3479P	7.92
MC3523U	5.80
MC4024P	12.78
MCT2	0.84
MCT61	1.18
MF10CCN	8.95
ML924	4.90
MM5309N	5.76
MM53105N	4.98
MM80C95N	1.44
MP7570JD	POA
MUX24EQ	9.60
MUX24FP	9.60
MV500DP	3.05
MV601DP	3.36
MV8870DP	5.52
NE5020N	10.84
NE527N	3.71
NE532N	0.60
NE536H	4.90
NE5530N	3.82
NE5532AN	1.58
NE5532N	0.80
NE5534AN	1.80
NE555N	0.20
NE556/SMD	0.70
NE556N	0.38
NE558N	2.28
NE564N	3.42
NE565N	2.94
NE567N	0.65
NE568N	POA
NE570N	4.60
NE571N	3.40
NE589N	4.25
NE592/SMD	1.80
NE592N	1.40
NE592N14	0.92
NE602AN	2.98
NE602N	2.40
NE604AN	8.24
NE605N	8.60
NE612AN	2.87
NJM4556D	1.20
NJM4558DX	1.20
OP07CJ	3.60
OP07CN	0.95
OP07CP	0.95
OP07EP	3.10
OP11GP	5.85
OP177FP	3.71
OP27GP	2.89
OP42FZ	7.44
OP77GP	2.07
OPO7CN	0.95
PM7548HP	18.20
RC4136N	0.98
RC4193N	POA
RC4194N	2.85
RC4207GN	1.92
RC4558	0.90
RC4558P	0.60
REF01CP	3.33
REF01HP	3.33
REF02CP	3.98
REF03GP	3.69
REF25Z	1.12
S2560A	POA
SAA1027	6.51
SAA1043P	7.98
SAA3049P	9.92
SAA5025D	7.65
SAA6002A	10.80
SAS560S	3.40
SED2000FVA	9.60
SFC2301ADC	6.78
SFC2741DC	0.18
SG3524N	4.60
SI7660CJ	1.92
SL1452	6.75
SL2364C	3.97
SL3117B	POA
SL486DP	2.98
SL490DP	2.80
SL560CDP	3.00
SL6270CDP	3.30
SL6700CDP	5.47
SN5281CN	POA
SN55451BJG	POA
SOC12	0.20
SP1648DG	5.53
SP4534	POA
SP4740DP	4.46
SP8629DP	3.44
SP8660DP	4.96
TA7215P	7.20
TA7256P	2.60
TA7368P	POA
TA7658P	POA
TA78005AP	POA
TA8200AH	POA
TA8410K	2.80
TA8449P	POA
TA8659AN	POA
TAA861A	POA
TBA120S	0.60
TBA240B	POA
TBA570	POA
TBA820MT	POA
TBA920	POA
TBA990	POA
TC9106BP	POA
TCA335A	POA
TCA965	POA
TCM1520AP	POA
TCM1531P	POA
TCM1705AN	POA
TCM3105N	9.42
TCM5087N	2.40
TCM5089N	2.40
TDA1083	2.60
TDA1085A	2.96
TDA1085C	3.80
TDA1151	1.10
TDA1170S	2.80
TDA1515A	4.98
TDA1521A	4.37
TDA1576	3.90
TDA1578A	3.60
TDA2595	3.32
TDA3048N	1.85
TDA3505	POA
TDA3810	POA
TDA440	POA
TDA4510	3.38
TDA4563	3.38
TDA4660	POA
TDA7010T	POA
TDA7052	2.52
TDA8702	6.22
TEA1045	POA
TEA1060	4.20
TEA5620	POA
TIPC2801KV	8.40
TL026CP	1.84
TL062CN	0.52
TL062CP	0.52
TL064CD	0.98
TL064CN	0.88
TL064ID/SMD	2.10
TL071ACP	1.84
TL071CP	0.64
TL072ACP	1.48
TL072CN	0.50
TL072CP	0.50
TL074ACN	2.85
TL074CN	0.84
TL081CP	0.48
TL082CP	0.48
TL084CN	0.48
TL27L2CD/SMD	1.98
TL497ACN	3.44
TL507CP	4.03
TL7702ACP	2.04
TL7705ACP	2.04
TL7705CP	2.04
TL7709ACP	2.04
TL7770-SC	3.82
TL783CKC	5.10
TLC2201CP	3.74
TLC2274CN	2.85
TLC251CP	2.54
TLC2652CP	4.92
TLC2654CP	4.84
TLC271CP	0.84
TLC272CP	1.30
TLC274CN	2.40
TLC339CN	1.98
TLC372CP	1.40
TLC551CP	3.68
TLC555CP	0.65
TLC556CN	1.58
TLC7524CN	5.24
TLE2061CP	2.20
TLE2062CP	3.40
TLE2064CN	3.45
TLE2161CP	2.42
TMS3477NL	5.96
TPIC2406NE	7.14
TPIC2802KV	8.40
TPIC6259N	3.28
TPIC6273N	3.28
TPIC6595N	3.28
TSC426CPA	POA
TSC500CPE	POA
TSC7106CPL	6.81
TSC7116CPL	5.25
TSC7126CPL	5.35
TSC766OCPA	1.40
U1096B	4.92
U2066B	2.64
U2400B	5.50
U664B	3.95
UA2240PC	1.40
UA709CP	0.85
UA709PC	0.85
UA715HC	4.50
UA723CP	0.70
UA733CJ	2.98
UA741MP	0.60
UA741TC	0.28
UA748CP	0.36
UA748TC	0.52
UA77000UIC	POA
UA798TC	3.80
UCN5800A	2.40
UCN5801A	2.60
UDN2981A	2.00
UDN2982A	2.00
UDN6118A	1.65
UGN3501M	POA
ULN2001AN	0.44
ULN2002A	0.44
ULN2003AN	0.44
ULN2004AN	1.40
ULN2024A	1.40
ULN2032A	1.40
ULN2803AN	0.84
UM5100	POA
UM5101	3.80
XR2211CP	POA
XTR110KP	9.95
Y1112/TI	4.60
ZN1445	POA
ZN414Z	1.04
ZN415E	1.84
ZN423	2.20
ZN425E-8	5.97
ZN426E-8	3.68
ZN428E-8	6.95
ZN429E-8	2.64
ZN449E	4.76

75 SERIES

75107	1.02
75107A	1.02
75108	1.80
75108A	1.84
75108B	2.08
75109A	2.46
75110A	1.36
75113	3.02
75114	3.04
75115	1.60
75116	3.30
75121	2.60
75122	POA
75136	3.10
75138	4.40
75140	2.65
75150	1.60
75150M	2.65
75152	6.36
75154	1.75
75154M	1.75
75155	1.20
75157	4.40
75159	5.45
75160A	5.95
75161A	6.47
75162A	7.59
75172NG	3.68
75173	3.68
75174	3.20
75174NG	3.68
75175	2.60
75176A	1.60
75176B	2.28
75176BT	4.98
75177	2.60
75178	2.60
75182	2.60
75183	2.60
75188	0.40
75189	0.85
75189A	0.85
75361	2.84
75365	2.72
75437A	3.26
75450B	0.64
75451	0.28
75451B	0.48
75452	0.28
75452B	0.48
75453	0.64
75453B	0.64
75454	0.64
75454B	0.98
75462	0.98
75463	1.10
75468	3.60
75469	1.30
75470	POA
75471	1.68
75472	1.48
75473	1.48
75474	2.25
75477	2.10
75491	0.68
75ALS176	2.88
75ALS192	2.88
75ALS193J	3.22
75C1154	2.88
75C1406	2.73
75C185	3.98
75C188	1.20
75C189A	1.32
75C189AD	1.32
75LBC176	2.60

TRANSISTORS THYRISTORS & TRIACS

40406	1.60
40673	2.40
BC107A/B	0.17
BC108A/B/C	0.17
BC109B/C	0.18
BC140-16	0.48
BC146/01	0.58
BC149	0.40
BC157	0.34
BC158	0.34
BC169C	0.14
BC179	0.24
BC182	0.08
BC182A	0.08
BC182B	0.08
BC182L	0.08
BC182LB	0.08
BC183	0.08
BC183C	0.08
BC183L	0.08
BC184	0.08
BC184B	0.08
BC184L	0.08
BC184LC	0.08
BC212-18	0.08
BC212A	0.08
BC212B	0.08
BC212L	0.08
BC212LB	0.08
BC213	0.08
BC213L	0.08
BC214	0.08
BC214L	0.11
BC237	0.08
BC239	0.12
BC307	0.08
BC327	0.08
BC328	0.08
BC337	0.08
BC337-25	0.08
BC489	0.24
BC490	0.30
BC516	0.22
BC517	0.20
BC546	0.05
BC546A	0.05
BC546B	0.05
BC547	0.08
BC547A	0.08
BC547B	0.08
BC547C	0.08
BC548	0.08
BC548B	0.08
BC549	0.08
BC549B	0.08
BC550	0.08
BC550B	0.08
BC550C	0.08
BC556	0.08
BC556A	0.08
BC556B	0.08
BC557	0.08
BC557B	0.08
BC558	0.08
BC558A	0.08
BC558B	0.08
BC559A	0.08
BC559B	0.08
BC560A	0.08
BC560C	0.08
BC184C	0.08
BCY71	0.22
BD131	0..88
BD135	0.44
BD241A	0.98
BD242C	0.52
BD243	0.50
BD516	0.78
BD675	0.52
BD676	0.52
BD679	0.54
BD680	0.56
BD743C	1.90
BDT85	1.12
BDX67B	2.78
BDY96	3.60
BF195-C	0.08
BF199	0.22
BF200	0.16
BF256B	0.38
BF256C	0.38
BF259	0.40
BF324	0.28
BF421	0.12
BF450	0.20
BF451	0.22
BF494	0.16
BF759	0.26
BF961	0.66
BF981	0.90
BF982	0.88
BFG65	1.79
BFR53-2GHz	0.48
BFR91-5GHz	0.90
BFR91A-6GHz	1.20
BFW10	1.20
BFX48	0.49
BFX85	0.59
BFX88	0.30
BFX89	1.59
BFY50	0.34
BFY52	0.34
BFY90	0.92
BS107	0.28
BS170	0.38
BS250	0.52
BSR60	0.48
BSX20	0.38
BSX21	0.48
BSX61	1.85
BT136-600	1.10
BUW46	4.94
BUZ11	1.60
BUZ11A	1.62
BUZ47A	6.90
IRFZ14	1.14
IRFZ20	1.77
J113	0.39
J175	0.68
J270	0.92
JA101	0.48
MBD501	1.10
MJE13070	1.10
MJE340	0.68
MJE350	1.10
MJE520	0.80
MPS3638	0.18
MPSA06	0.12
MPSA13	0.12
MPSA63	0.32
MPSA92	0.24
MPSU05	2.21
MTP8P08	2.80
OC147	1.80
OC19	1.85
OC45	0.65
OC72	0.80
OC78	0.80
OC81M	0.80
OC81Z	0.92
PN3643	0.18
TIC106M	0.78
TICP206D	0.61
TICV106D	0.24
TIP115	0.55
TIP121	0.68
TIP145	1.37
TIP2955	0.88
TIP30	0.48
TIP3055	0.88
TIP31A	0.38
TIP32A	0.40
TIP47	0.80
V275LA10	0.92
VN0104N3	0.92
VN66AFD	1.40
VN90AB	2.96
VP0104-N3	0.92
VP0104N2	0.98
VP0104N3	0.92
ZTX212	0.18
ZTX237	0.26
ZTX300	0.18
ZTX313L	0.28
ZTX320	0.38
ZTX510	0.18

IC SOCKETS LOW PROFILE

No. of Pins	Pin spac-ing	Gold Turn Pin	Tin sldr Tail	Gold sldr Tail
6	0.3	18p	6p	18p
8	0.3	18p	6p	18p
14	0.3	31p	8p	31p
16	0.3	33p	10p	33p
18	0.3	39p	11p	39p
20	0.3	45p	12p	45p
22	0.3	54p	14p	
24	0.3	54p	14p	
24	0.6	54p	14p	
28	0.6	60p	16p	
32	0.6	65p	22p	
40	0.6	70p	22p	
48	0.6	85p		
64	0.75	260p		
64	0.9	260p		

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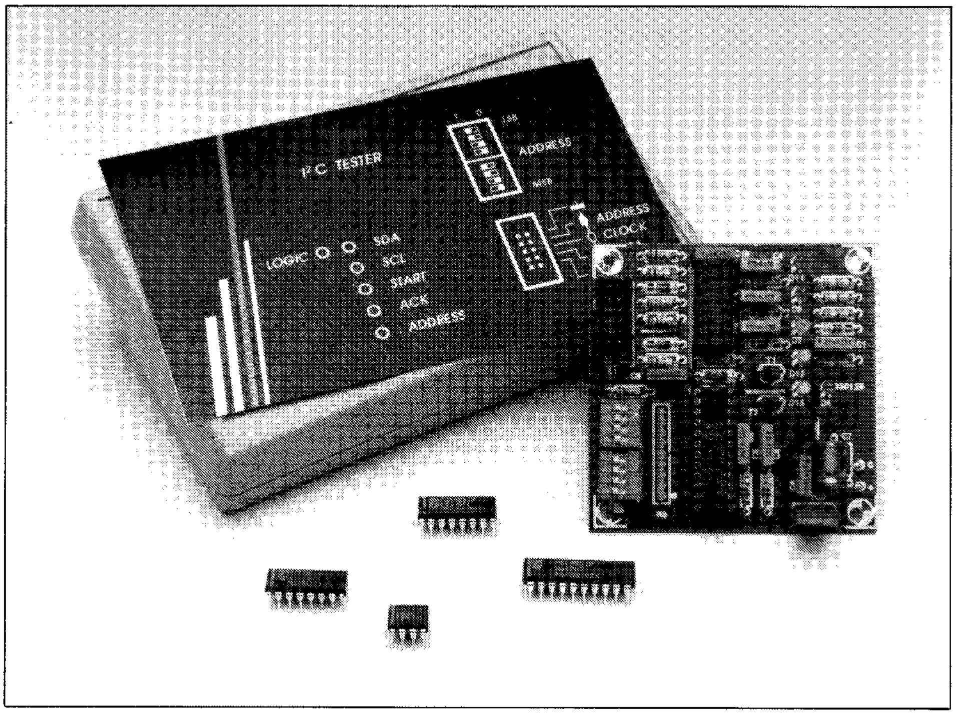
I^{2}C TESTER

There can be no doubt that the I^{2}C bus has become the *de facto* standard for communication between ICs in audio and video equipment. The three wire bus, invented by Philips, provides an intelligent way of exchanging data between the increasingly complex ICs in such equipment. Normally, an oscilloscope or a logic analyser is used to test the functions in an I^{2}C system. Since an oscilloscope is sometimes inadequate, and a logic analyser costly or not available, a good, low-cost alternative to these instruments is described in this article.



Design by W. Foede

THE I^{2}C system has been with us for several years now, and has been the subject of a number of articles in *Elektor Electronics*. Following the description of an interface circuit that enables a PC to take control of an I^{2}C bus, a number of extension circuits were published for various applications (see the I^{2}C publications overview at the end of this article).

Nowadays, there exists an I^{2}C compatible IC for almost any application in consumer electronics equipment. If a fault occurs in a piece of equipment fitted with I^{2}C ICs, it is often necessary to test the bus and the components connected to it. In most cases, it is possible to use an oscilloscope for a basic test. Unfortunately, the scope will only tell you if there are signals on the SDA and SCL lines (high level: bus is free; alternating voltage: data and/or clock present), no more, no less. For a more extensive test you need a special tester, and that is described here.

The present I^{2}C bus tester has a number of LEDs and DIP switches that tell you exactly what is happening on the I^{2}C bus. The instrument allows an IC address to be set, and can be 'armed' to see if this address appears on the bus. Further, it allows the general data traffic to be monitored. There are six LEDs which provide the following indications:

SDA/SCL: data present on SDA or SCL;
START: valid start condition is being transmitted;
ACK: hexadecimal address set on the tester is confirmed by the relevant slave IC (with an ACK pulse);
ADDRESS: hexadecimal address set with the aid of the DIP switches is present on the bus;
LOGIC: static logic level on a line; independent of the I^{2}C bus.

In principle, such test data could be made visible on a logic analyser, but that soon becomes problematic if there are several slave ICs on a bus. Moreover, the logic analyser is a costly instrument which is rarely seen in a hobbyist's workshop. None the less, if you are the fortunate owner of a logic analyser, the I^{2}C tester offers an additional output supplying the ADDRESS signal, which enables the logic analyser to be triggered on certain addresses. Since only two relatively slow data streams are to be visualized, an alternative would be to use a digital oscilloscope (whose external synchronization input is connected to the ADDRESS output on the I^{2}C tester).

Heart of the circuit: a GAL

At the heart of the circuit is a GAL (generic array logic) Type 6001. It contains a large number of logic functions needed for the I^{2}C tester, and thus keeps the component count in the circuit to a minimum. Although the 6001 looks similar to the 20V8 which has been used before in *Elektor Electronics* projects, its internal structure is far more intricate, offering more possibilities. The most important extra features are:

- 10 instead of 8 In/Out macro cells IOLMC (pins 14 through 23). Eight 'hidden' macro cells BLMC (not bonded out to pins).
- The number of product terms allowed on one output is only restricted by the total number of 74.
- Each macro cell can be clocked individually with a product term (asynchronous clocking).
- All macro cells can be reset simultaneously (asynchronous reset).
- Eight IN macro cells ILMC (pins 2 through 11) (not used here).

The above additional features are fully exploited in the present design, hence the choice of the 6001 in favour of the 20V8.

Defining the desired GAL functions

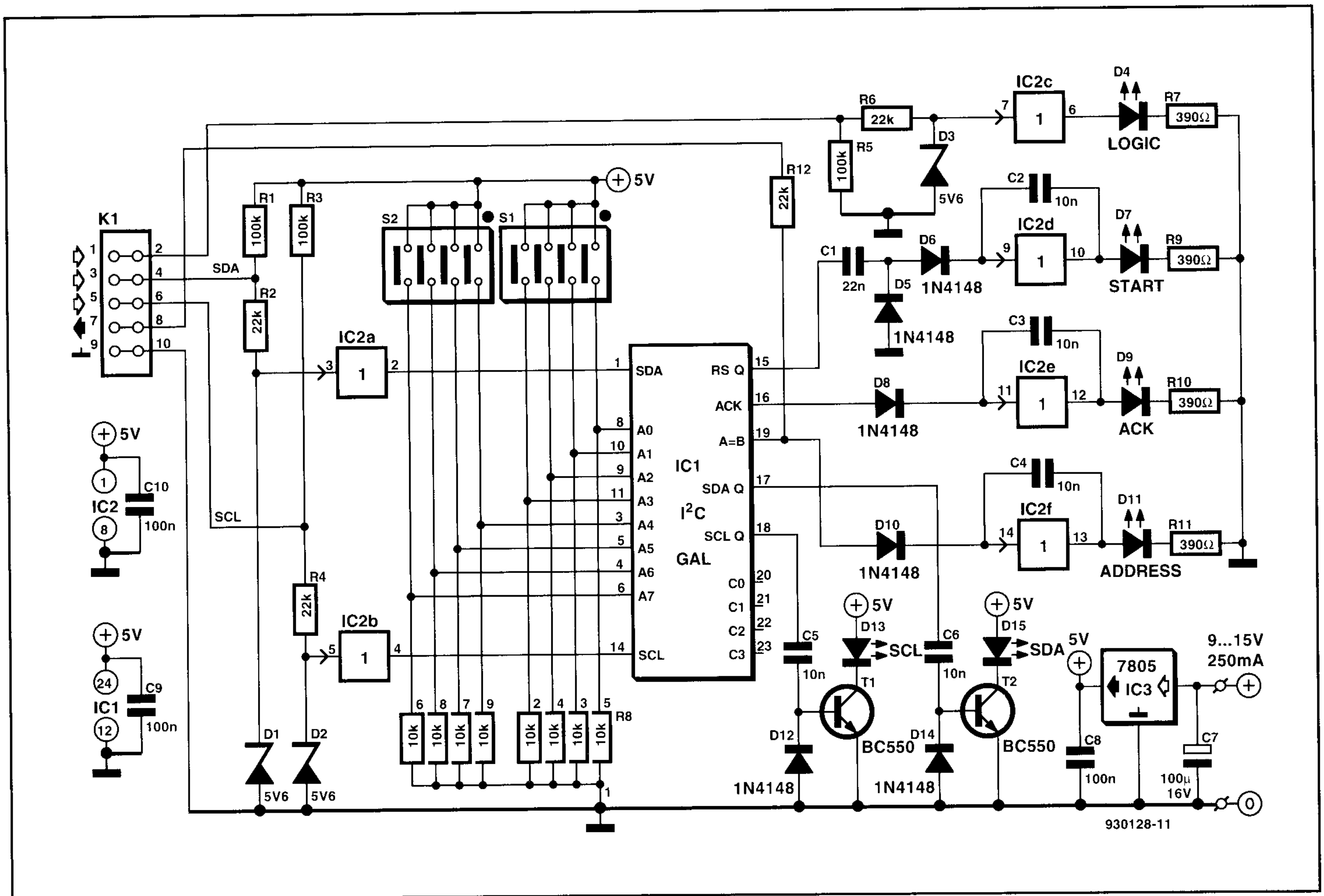


Fig. 1. Not much of a circuit diagram, really, this one of the I²C tester, but bear in mind the complexity of the circuitry contained in the GAL, circuit IC1.

with 'bare hands' is a pretty arduous task. Fortunately, a number of affordable computer programs are available these days that come to your rescue. In this case, the author made use of the program 'easy ABEL'. This program allows you to describe the design in general terms with the aid of a Hardware Description Language, whereupon the program compiles the optimized functions, and in addition suggests ICs for that purpose. After the IC selection, pins are automatically assigned to the different functions. The result is a JEDEC programming file which can be read by most GAL programmers to burn the design into a GAL. Not to worry if you do not have a GAL programmer, because the GAL used in the present circuit comes ready-programmed through our Readers Services (see p. 70).

Two ICs and a power supply

Looking at the circuit diagram of the I²C tester, **Fig. 1**, you may feel a little disappointed because it is so simple. Well, that is because so many functions are implemented in the GAL. Apart from the 6001, only a few buffers are required to complete the circuit. The buffers being contained in a single CD4050, the total number of logic ICs in the circuit is ... two!

The internal diagram of the programmed GAL used in the present circuit is given in **Fig. 2**. Obviously, the circuit would have been a lot more

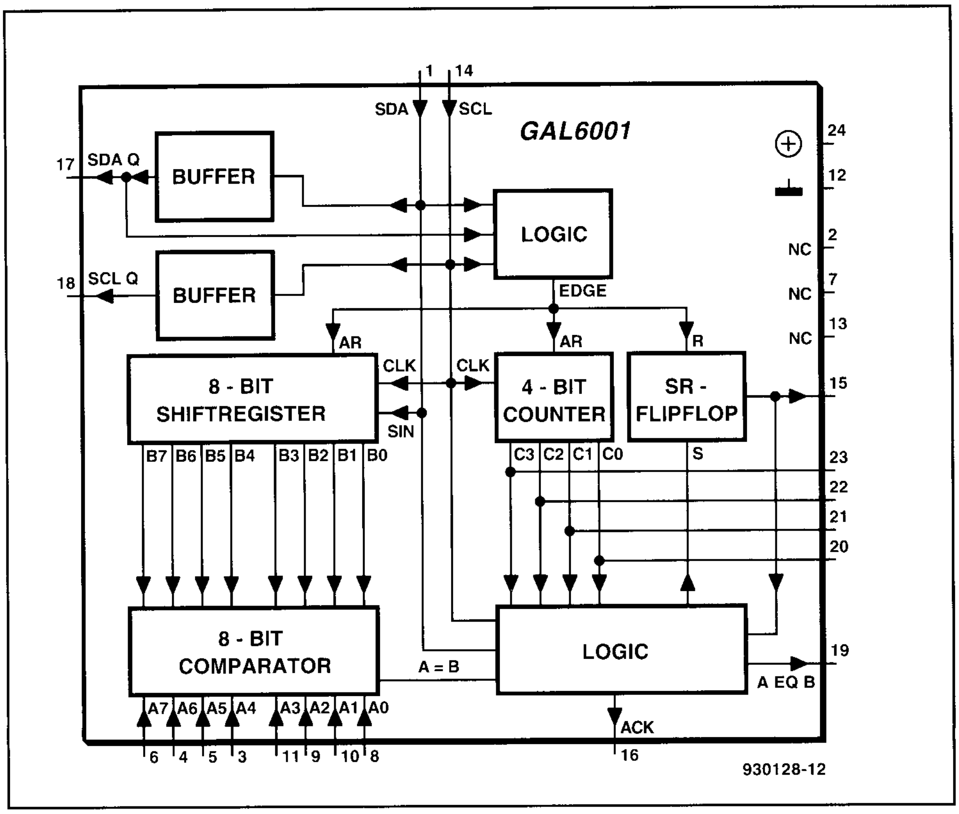


Fig. 2. Block schematic representation of the functions contained in GAL Type 6001.

complex and difficult to build if all the functions shown were realized using standard logic ICs.

The operation of the circuit will be explained with reference to the circuit diagram (**Fig. 1**) and the timing diagram shown in **Fig. 3**. Signals SDA (serial data) and SCL (serial clock) arrive on connector K_1. Zener diodes D_1 and D_2 reduce any excessive input voltage levels to about 5.6 V (the normal supply voltage in an I^2C system is 5 V). Next, the signals are 'cleaned' by buffers IC_{2a} and IC_{2b}, whereupon they are taken to pins 1 and 14 of the GAL. Inside the GAL, the SDA and SCL signals are buffered again, and then sent to two LED drivers, T_1 and T_2, via pins 17 and 18. Capacitors C_5 and C_6 ensure that the LEDs light on the positive SDA and SCL signal edges only.

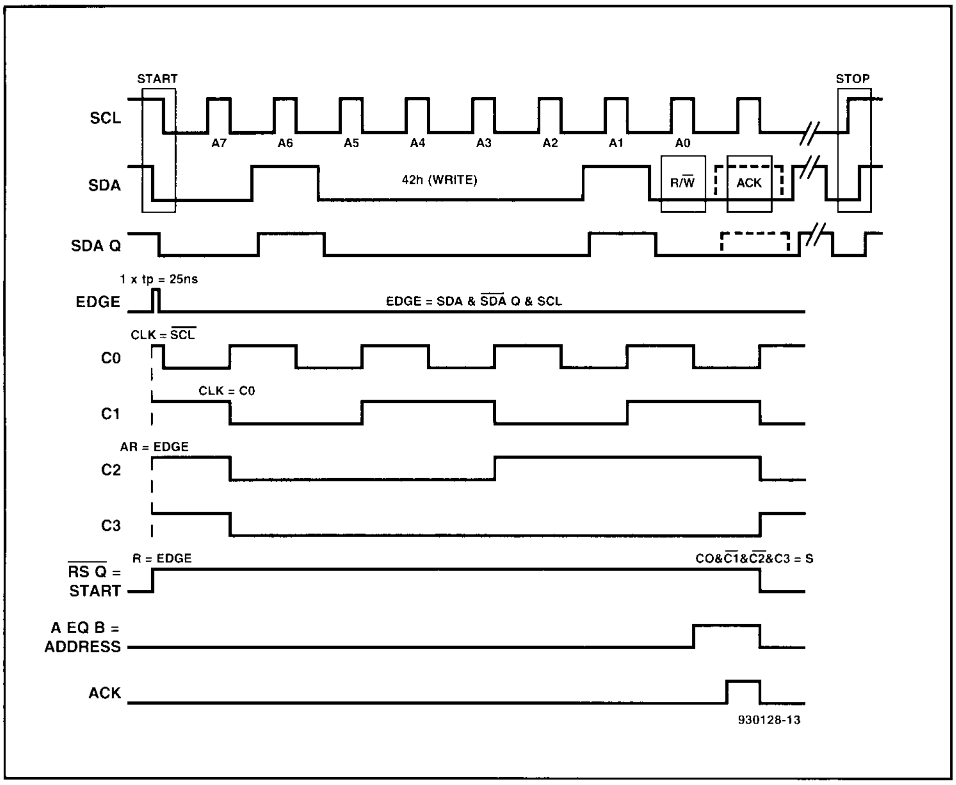
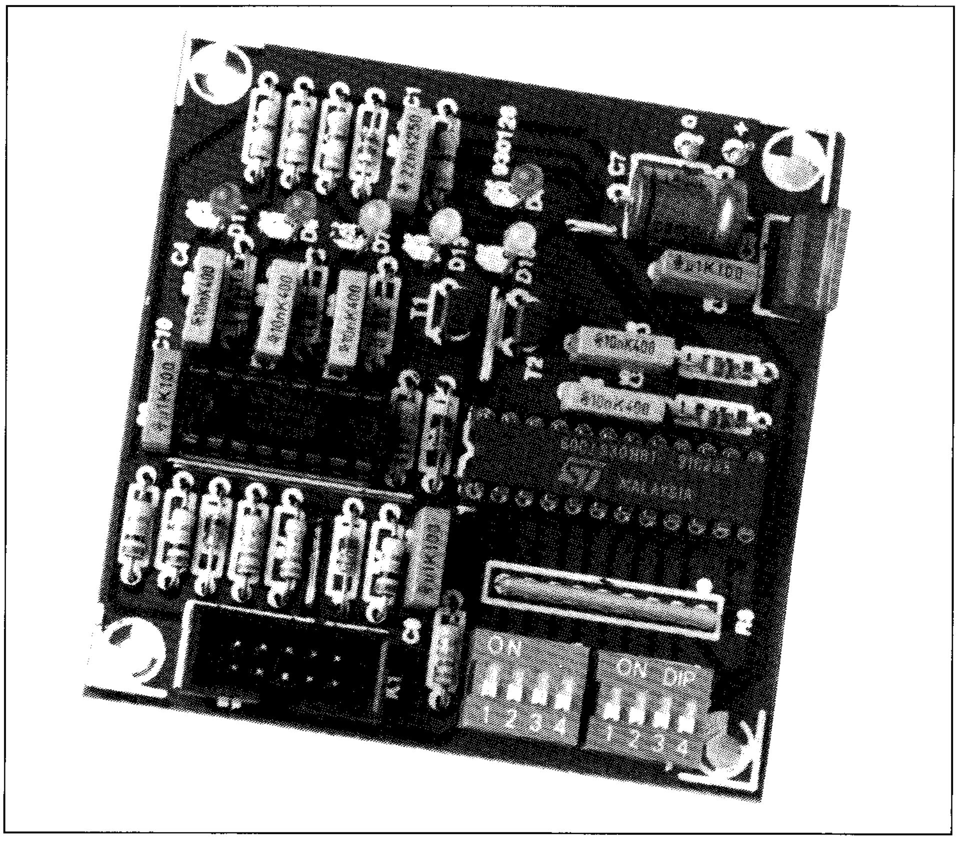


Fig. 3. This timing diagram shows what happens to the signals that enter the GAL

A start condition on the I^2C bus is recognized by a small logic circuit shown at the right in Fig. 2. This subcircuit supplies the signal called 'edge', which is generated the moment SDA goes low when SCL is high. The 'edge' signal starts the read cycle of an 8-bit shift register, and resets a 4-bit counter. It is also used to reset an S-R bistable. Clocked by the SCL signal, the shift register turns the serial address transmitted via the SDA line (7-bit address + R/W bit) into an 8-bit parallel word. In the block diagram, the most significant bit (MSB) is at the far left on the shift register outputs. The first seven received bits form the address, while the eighth bit indicates the data direction. A '0' means: master ready to send data (write). A '1' means: master ready to receive data (read). The shift register outputs are connected to an 8-bit comparator circuit which also reads the bit combination set on two 4-way DIP switches, S_1 and S_2. When the received address matches that set on the DIP switches, the comparator supplies a 'match' signal to the logic section shown in the lower right-hand corner of the block diagram.

The bistable and the 4-bit counter are added to ascertain that the byte detected by the comparator is actually the address byte. This double check is necessary because the same bit pattern may be conveyed while data is being written. The bistable and the counter are reset by the 'edge' signal (which appears after the start condition), whereupon the 4-bit counter is clocked by the SCL signal. The bistable is set again by the logic during the nine pulses following the start condition. The three outputs 15, 16 and 19 are connected to three buffers (IC_{2d}, IC_{2e} and IC_{2f}) which are 'shunted' by capacitors to make them function as monostable multivibrators. This is necessary because pins 16 and 19 supply 'short' pulses. In this way, the LEDs connected to the circuit outputs light long enough to ensure a clear indication. On output 15, C_1 and D_5 ensure that rising (positive) pulse edges are made visible.

Correct reception of a byte addressed to a particular IC is acknowledged by that IC returning an ACK pulse. The transmitter (in this case the master IC) pulls the SDA line high, and waits for the slave IC to pull it low again. If that does not happen, the communication between the two ICs is stopped. The ACK LED lights if the adress byte is acknowledged by the slave IC. In that case, you may safely assume that the slave IC is functional (that is, the I^2C communication section in the IC).



COMPONENTS LIST

Resistors:
R1;R3;R5 = 100kΩ
R2;R4;R6;R12 = 22kΩ
R7;R9;R10;R11 = 390Ω
R8 = 8-way resistor array 10kΩ

Capacitors:
C1 = 22nF
C2-C6 = 10nF
C7 = 100µF/16V
C8;C9;C10 = 100nF

Semiconductors:
D1;D2;D3 = 5V6/400mW zener diode
D4;D9;D11 = LED red, 3mm
D5;D6;D8;D10;D12;D14 = 1N4148
D7 = LED green, 3mm
D13;D15 = LED yellow, 3mm
T1;T2 = BC550
IC1 = GAL6001 (order code 6341; see page 70)
IC2 = 4050
IC3 = 7805

Miscellaneous:
K1 = 10-way straight boxheader.
S1;S2 = 4-way DIP switch.
Printed circuit board and programmed GAL. Set code: 930128 (see page 70).
1 off Mains adaptor 9-15V/250 mA.

The remaining buffer, IC_{2C}, is used to make a simple logic tester that allows logic levels to be made visible. As on the SDA and SCL inputs, a protection is provided that limits the input voltage to about 5.6 V.

The power supply is conventional, consisting of a 7805 three-pin fixed voltage regulator and the usual decoupling capacitors for noise suppression. The mains transformer is connected externally. In fact, it is contained in a mains adaptor with an output voltage of 9-15V a.c. This is a safe as well as economical solution to the mains transformer problem.

Construction

The tester is simple to build on the printed circuit board shown in **Fig. 4**. This board is available ready-made through our Readers Services. Construction is straightforward using the component overlay printed on the board. The GAL is best fitted last, so that it can not be damaged when the other components are soldered.

The front panel (**Fig. 5**) is designed such that the function of the LEDs and the switches are clearly indicated. Pay attention to the depth of the enclosure you are using when mounting the LEDs, the DIP switches and the 10-pin header, K_1. Obviously, the LEDs must

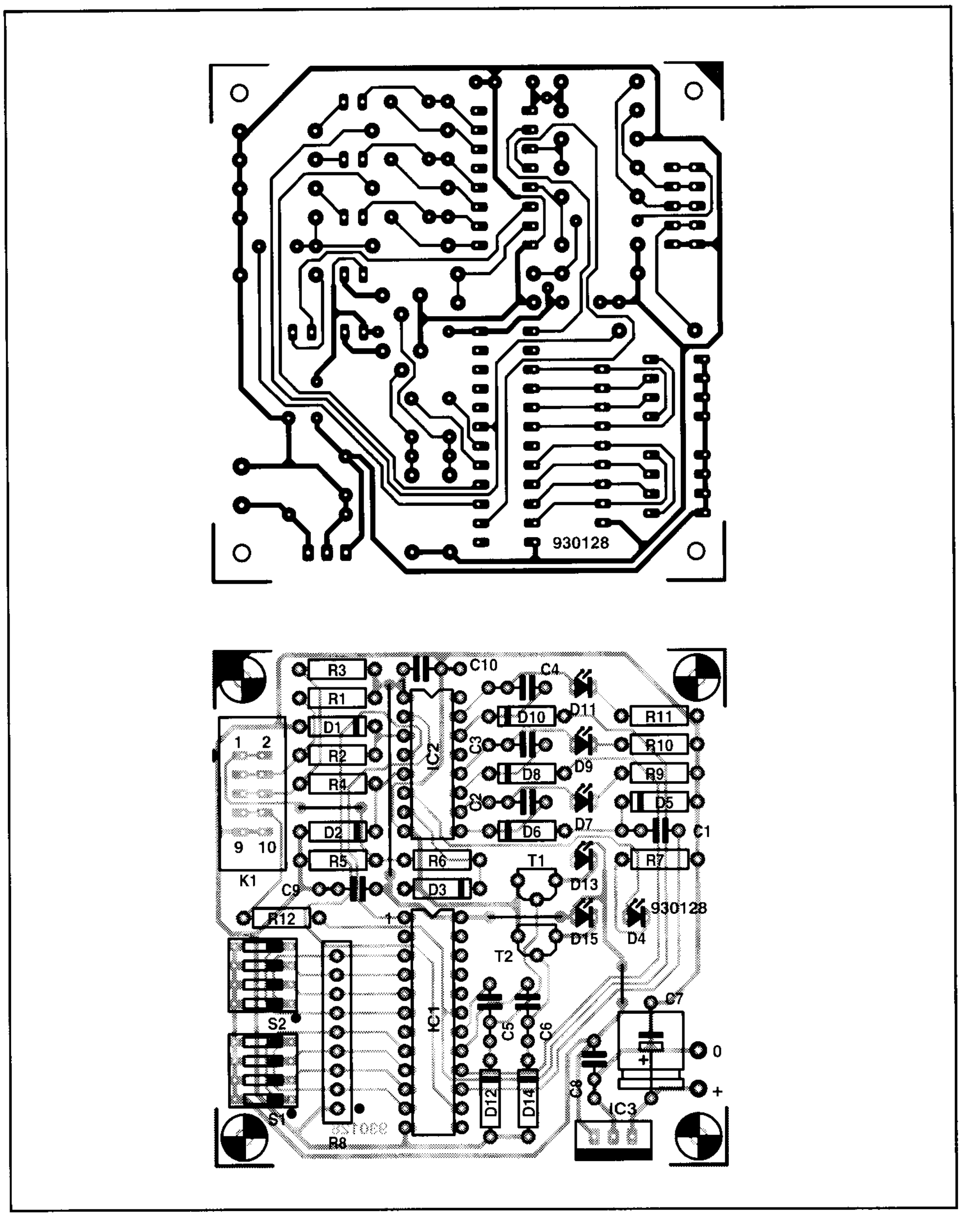
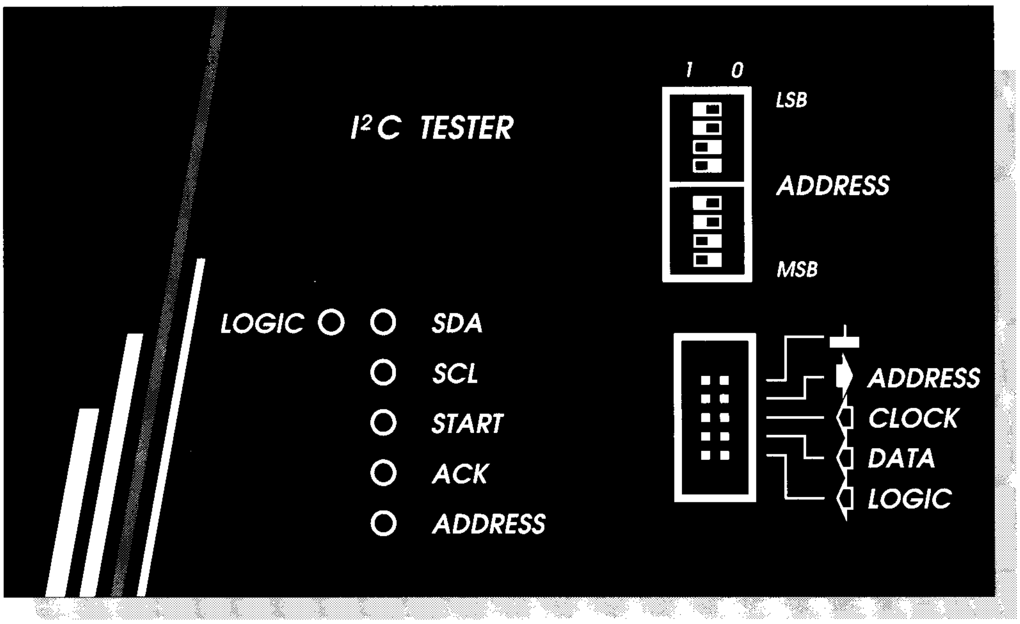


Fig. 4. Artwork for the printed circuit board designed for the I²C tester.



930128-F

Fig. 5. Suggested front panel layout of the I²C tester.

be fitted just behind the front panel, while the DIP switches and the header should be accessible, which means that they are mounted at least level with the top side of the front panel. Fortunately, that is easy to achieve by mounting the printed circuit board behind the front panel, using PCB spacers (stand-offs) of the right length.

The power supply socket is fitted into a side panel of the enclosure. The type of socket depends on the mains adaptor used.

Finally, make a 'test cable'. This consists of a piece of 10-way flatcable (about 50 cm long), fitted with a 10-way IDC (press-on) socket at one side, and miniature test clips at the other. The test clips should be labelled to avoid confusion about their connection in the circuit under test.

The tester is then ready for measurements on I²C circuits of almost any complexity. One problem you may be faced with during such measurements is that the addresses of the ICs on the bus are not known. Although the base addresses of most I²C ICs are fixed by the manufacturer, the designer of the circuit still has the freedom to determine part of the actual address with the aid of certain IC pins. It is, therefore, desirable to have handy as much data on the ICs as possible, and, preferably, also a circuit diagram of the equipment under examination. To help you on the way, the addresses of a wide range of I²C ICs from Philips Semiconductors are shown in **Table 1**. Unfortunately, when you encounter ICs whose address is not clearly recognizable, there is no other alternative than to try a couple of different device addresses using the DIP switches, to see if the IC responds at all to master read/write operations. ■

Previous I²C projects in this magazine:

Inter-IC communications, September 1990
Video digitizer, July/August 1991.
I²C interface for PCs, February 1992.
I²C LED display,June 1992.
Speech/sound memory, December 1992.
I²C alphanumerical display, July/August 1993.
I²C bus fuse, July/August 1993.
I²C opto/relay card, February 1993,
I²C power switch, December 1993.

Type	Function	Address
n.a.	'general call' address	0 0 0 0 0 0 0 X
n.a.	reserved addresses	0 0 0 0 Y Y Y X
		1 1 1 1 Y Y Y X
PCD3311/12	DTMF/modem/tone generator	0 1 0 0 1 0 A1 X
PCF8200	speech synthesizer	0 0 1 0 0 0 0 X
PCF8566	universal LCD driver	0 1 1 1 1 1 A1 X
PCF8570/71	static RAM (256x8/128x8)	1 0 1 0 A3 A2 A1 X
PCF8570C	static RAM (256x8)	1 0 1 1 A3 A2 A1 X
PCF8572	EEPROM (128x8)	1 0 1 0 A3 A2 A1 X
PCF8573	realtime clock/calendar	1 1 0 1 0 A2 A1 X
PCF8574	remote 8-bit I/O-expander	0 1 0 0 A3 A2 A1 X
PCF8574A	remote 8-bit I/O-expander	0 1 1 1 A3 A2 A1 X
PCF8576	universal LCD driver	0 1 1 1 0 0 A1 X
PCF8577	LCD direct/duplex driver	0 1 1 1 0 1 0 X
PCF8577A	LCD direct/duplex driver	0 1 1 1 0 1 1 X
PCF8578	LCD-driver for dot matrix	0 1 1 1 1 0 A1 X
PCF8579	LCD-driver for dot matrix	0 1 1 1 1 0 A1 X
PCF8582A	EEPROM (256x8)	1 0 1 0 A3 A2 A1 X
PCF8583	clock/calendar w. static RAM	1 0 1 0 0 0 A1 X
PCF8591	8-bit A/D and D/A converter	1 0 0 1 A3 A2 A1 X
SAA1064	4-digit LED driver	0 1 1 1 0 A2 A1 X
SAA1136	PCM audio interface	0 0 1 1 1 1 0 X
SAA1300	tuner switching circuit	0 1 0 0 0 A2 A1 X
SAA3028	IR transcoder (RC-5)	0 1 0 0 1 1 0 X
SAA4700	VPS dataline processor	0 0 1 0 0 0 A1 X
SAA5243/45	comp. controlled teletext circuit	0 0 1 0 0 0 1 X
SAA9020	memory controller	0 0 1 0 1 A2 A1 X
SAA9050/51	dig. multistandard TV-decoder	1 0 0 0 1 0 1 X
SAA9055P/8A	dig. SECAM decoder	1 0 0 0 1 0 1 X
SAA9055P/8E	dig. SECAM decoder	1 0 0 0 1 1 1 X
SAA9062/63/64	dig. deflection controller	1 0 0 0 1 1 0 X
SAA9068	picture-in-picture controller	0 0 1 0 0 1 A1 X
SAB3035/36/37	comp. tuning interface	1 1 0 0 0 A2 A1 X
SAF1135	data line decoder	0 0 1 0 0 A2 A1 X
TDA8370	TV sync processor	1 0 0 0 1 1 0 X
TDA8400	comp. interface prescaler synth.	1 1 0 0 0 A2 A1 X
TDA8405	stereo TV sound processor	1 0 0 0 0 1 0 X
TDA8420/8421	stereo audio processor	1 0 0 0 0 0 A1 X
TDA8425	stereo audio processor	1 0 0 0 0 0 1 X
TDA8440	video/audio switch	1 0 0 1 A3 A2 A1 X
TDA8442	colour decoder interface	1 0 0 0 1 0 0 X
TDA8443A	YUV/RGB interface	1 1 0 1 A3 A2 A1 X
TDA8444	8-fold 6-bit DAC	0 1 0 0 A3 A2 A1 X
TDA8461	PAL/NTSC decoder	1 0 0 0 1 0 A1 X
TDA8440	switch for TV receivers	1 0 0 1 A3 A2 A1 X
TEA6000/6100	FM/IF system and µP tuner	1 1 0 0 0 0 1 X
TEA6300(T)/10T	sound fader circuit	1 0 0 0 0 0 0 X
TEA6330T	control amplifier	1 0 0 0 0 0 0 X
TEA6360	equalizer	1 0 0 0 0 1 A1 X
TSA5510(T)	1.3-GHz frequency synthesizer	1 1 0 0 0 A2 A1 X
TSA6057(T)	radio PLL frequency synthesizer	1 1 0 0 0 1 A1 X
UMA1000T	data processor for cordless tel.	1 1 0 1 1 A2 A1 X
UMA1010T	un. synthesizer for radio comm.	1 1 0 0 0 0 A1 X

A3, A2 or A1 = user-programmable address bit.
X = R/W bit (1 = read; 0 = write).
Y = don't care.

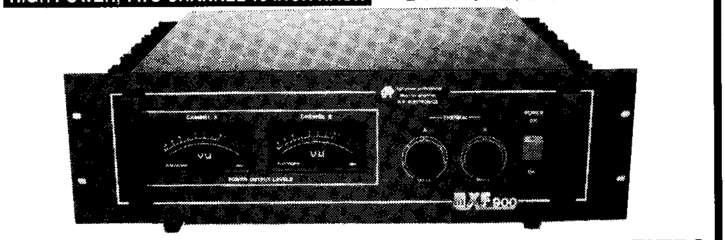
Table 1. Overview of I²C integrated circuits and their bus addresses (courtesy Philips Semiconductors).

POWER AMPLIFIER MODULES-TURNTABLES-DIMMERS-LOUDSPEAKERS-19 INCH STEREO RACK AMPLIFIERS

★ PRICES INCLUDE V.A.T. ★ PROMPT DELIVERIES ★ FRIENDLY SERVICE ★ LARGE (A4) S.A.E., 60p STAMPED FOR CATALOGUE ★

OMP MOS-FET POWER AMPLIFIERS HIGH POWER, TWO CHANNEL 19 INCH RACK

THOUSANDS PURCHASED BY PROFESSIONAL USERS



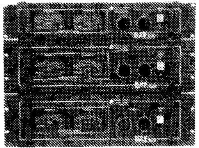
THE RENOWNED MXF SERIES OF POWER AMPLIFIERS

FOUR MODELS:- MXF200 (100W + 100W) **MXF400** (200W + 200W) **MXF600** (300W + 300W) **MXF900** (450W + 450W)

ALL POWER RATINGS R.M.S. INTO 4 OHMS, BOTH CHANNELS DRIVEN

FEATURES: ★Independent power supplies with two toroidal transformers ★ Twin L.E.D. Vu meters ★ Level controls ★ Illuminated on/off switch ★ XLR connectors ★ Standard 775mV inputs ★ Open and short circuit proof ★ Latest Mos-Fets for stress free power delivery into virtually any load ★ High slew rate ★ Very low distortion ★ Aluminium cases ★ MXF600 & MXF900 fan cooled with D.C. loudspeaker and thermal protection.

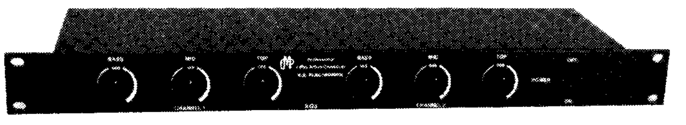
USED THE WORLD OVER IN CLUBS, PUBS, CINEMAS, DISCOS ETC.



SIZES:- MXF200 **W19″xH3½″ (2U)xD11″**
MXF400 **W19″xH5¼″ (3U)xD12″**
MXF600 **W19″xH5¼″ (3U)xD13″**
MXF900 **W19″xH5¼″ (3U)xD14¾″**

PRICES:- MXF200 £175.00 MXF400 £233.85
MXF600 £329.00 MXF900 £449.15
SPECIALIST CARRIER DEL. £12.50 EACH

OMP XO3 STEREO 3-WAY ACTIVE CROSS-OVER



Advanced 3-Way Stereo Active Cross-Over, housed in a 19" x 1U case. Each channel has three level controls: bass, mid & top. The removable front fascia allows access to the programmable DIL switches to adjust the cross-over frequency: Bass-Mid 250/500/800Hz, Mid-Top 1.8/3/5KHz, all at 24dB per octave. Bass invert switches on each bass channel. Nominal 775mV input/output. Fully compatible with OMP rack amplifier and modules.

Price £117.44 + £5.00 P&P

STEREO DISCO MIXER SDJ3400SE

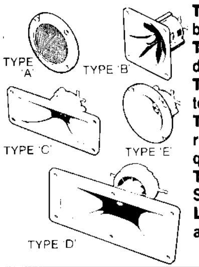
★ ECHO & SOUND EFFECTS★

STEREO DISCO MIXER with 2 x 7 band L & R graphic equalisers with bar graph LED Vu meters. **MANY OUTSTANDING FEATURES:- including Echo with repeat & speed control, DJ Mic with talk-over switch, 6 Channels with individual faders plus cross fade, Cue Headphone Monitor. 8 Sound Effects. Useful combination of the following inputs:- 3 turntables (mag), 3 mics, 5 Line for CD, Tape, Video etc.**

Price £144.99 + £5.00 P&P **SIZE: 482 x 240 x 120mm**

PIEZO ELECTRIC TWEETERS - MOTOROLA

Join the Piezo revolution! The low dynamic mass (no voice coil) of a Piezo tweeter produces an improved transient response with a lower distortion level than ordinary dynamic tweeters. As a crossover is not required these units can be added to existing speaker systems of up to 100 watts (more if two are put in series. **FREE EXPLANATORY LEAFLETS ARE SUPPLIED WITH EACH TWEETER.**



TYPE 'A' (KSN1036A) 3" round with protective wire mesh. Ideal for bookshelf and medium sized Hi-Fi apeakers. **Price £4.90 + 50p P&P.**

TYPE 'B' (KSN1005A) 3½" super horn for general purpose speakers, disco and P.A. systems etc. **Price £5.99 + 50p P&P.**

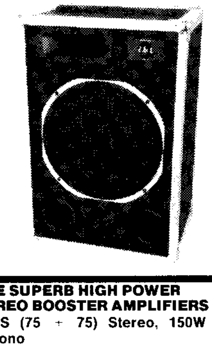
TYPE 'C' (KSN1016A) 2"x5" wide dispersion horn for quality Hi-Fi systems and quality discos etc. **Price £6.99 + 50p P&P.**

TYPE 'D' (KSN1025A) 2"x6" wide dispersion horn. Upper frequency response retained extending down to mid-range (2KHz). Suitable for high quality Hi-Fi systems and quality discos. **Price £9.99 + 50p P&P.**

TYPE 'E' (KSN1038A) 3¾" horn tweeter with attractive silver finish trim. Suitable for Hi-Fi monitor systems etc. **Price £5.99 + 50p P&P.**

LEVEL CONTROL Combines, on a recessed mounting plate, level control and cabinet input jack socket. 85x85mm. **Price £4.10 + 50p P&P.**

ibl FLIGHT CASED LOUDSPEAKERS



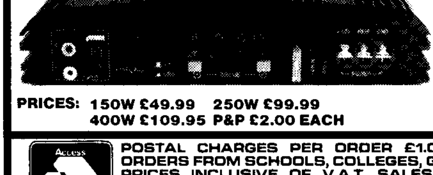
A new range of quality loudspeakers, designed to take advantage of the latest speaker technology and enclosure designs. Both models utilize studio quality 12" cast aluminium loudspeakers with factory fitted grilles, wide dispersion constant directivity horns, extruded aluminium corner protection and steel ball corners, complimented with heavy duty black covering. The enclosures are fitted as standard with top hats for optional loudspeaker stands.

POWER RATINGS QUOTED IN WATTS RMS FOR EACH CABINET
FREQUENCY RESPONSE FULL RANGE 45Hz - 20KHz

***ibl* FC 12-100WATTS (100dB) PRICE £159.00 PER PAIR**
***ibl* FC 12-200WATTS (100dB) PRICE £175.00 PER PAIR**
SPECIALIST CARRIER DEL. £12.50 PER PAIR

OPTIONAL STANDS PRICE PER PAIR £49.00
Delivery £6.00 per pair

IN-CAR STEREO BOOSTER AMPS



THREE SUPERB HIGH POWER CAR STEREO BOOSTER AMPLIFIERS

150 WATTS (75 + 75) Stereo, 150W Bridged Mono
250 WATTS (125 + 125) Stereo, 250W Bridged Mono
400 WATTS (200 + 200) Stereo, 400W Bridged Mono
ALL POWERS INTO 4 OHMS

Features:
★ Stereo, bridgable mono ★ Choice of high & low level inputs ★ L & R level controls ★ Remote on-off ★ Speaker & thermal protection.

PRICES: 150W £49.99 250W £99.99
400W £109.95 P&P £2.00 EACH

POSTAL CHARGES PER ORDER £1.00 MINIMUM. OFFICIAL ORDERS FROM SCHOOLS, COLLEGES, GOVT. BODIES, PLCs ETC. PRICES INCLUSIVE OF V.A.T. SALES COUNTER. VISA AND ACCESS ACCEPTED BY POST, PHONE OR FAX.

OMP MOS-FET POWER AMPLIFIER MODULES

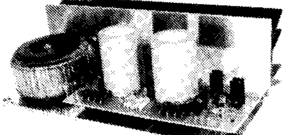
SUPPLIED READY BUILT AND TESTED.

These modules now enjoy a world-wide reputation for quality, reliability and performance at a realistic price. Four models are available to suit the needs of the professional and hobby market i.e. Industry, Leisure, Instrumental and Hi-Fi etc. When comparing prices, NOTE that all models include toroidal power supply, integral heat sink, glass fibre P.C.B. and drive circuits to power a compatible Vu meter. All models are open and short circuit proof.

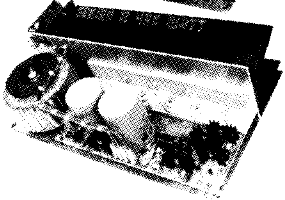
THOUSANDS OF MODULES PURCHASED BY PROFESSIONAL USERS

OMP/MF 100 Mos-Fet Output power 110 watts R.M.S. into 4 ohms, frequency response 1Hz - 100KHz -3dB, Damping Factor >300, Slew Rate 45V/uS, T.H.D. typical 0.002%, Input Sensitivity 500mV, S.N.R. -110 dB. Size 300 x 123 x 60mm.
PRICE £40.85 + £3.50 P&P

OMP/MF 200 Mos-Fet Output power 200 watts R.M.S. into 4 ohms, frequency response 1Hz - 100KHz -3dB, Damping Factor >300, Slew Rate 50V/uS, T.H.D. typical 0.001%, Input Sensitivity 500mV, S.N.R. -110 dB. Size 300 x 155 x 100mm.
PRICE £64.35 + £4.00 P&P



OMP/MF 300 Mos-Fet Output power 300 watts R.M.S. into 4 ohms, frequency response 1Hz - 100KHz -3dB, Damping Factor >300, Slew Rate 60V/uS, T.H.D. typical 0.001%, Input Sensitivity 500mV, S.N.R. -110 dB. Size 330 x 175 x 100mm.
PRICE £81.75 + £5.00 P&P

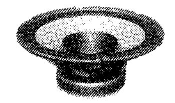


OMP/MF 450 Mos-Fet Output power 450 watts R.M.S. into 4 ohms, frequency response 1Hz - 100KHz -3dB, Damping Factor >300, Slew Rate 75V/uS, T.H.D. typical 0.001%, Input Sensitivity 500mV, S.N.R. -110 dB, Fan Cooled, D.C. Loudspeaker Protection, 2 Second Anti-Thump Delay. Size 385 x 210 x 105mm.
PRICE £132.85 + £5.00 P&P

OMP/MF 1000 Mos-Fet Output power 1000 watts R.M.S. into 2 ohms, 725 watts R.M.S. into 4 ohms, frequency response 1Hz - 100KHz -3dB, Damping Factor >300, Slew Rate 75V/uS, T.H.D. typical 0.002%, Input Sensitivity 500mV, S.N.R. -110 dB, Fan Cooled, D.C. Loudspeaker Protection, 2 Second Anti-Thump Delay. Size 422 x 300 x 125mm.
PRICE £259.00 + £12.00 P&P

NOTE: MOS-FET MODULES ARE AVAILABLE IN TWO VERSIONS: STANDARD - INPUT SENS 500mV, BAND WIDTH 100KHz. PEC (PROFESSIONAL EQUIPMENT COMPATIBLE) - INPUT SENS 775mV, BAND WIDTH 50KHz. ORDER STANDARD OR PEC.

LOUDSPEAKERS



LARGE SELECTION OF SPECIALIST LOUDSPEAKERS AVAILABLE, INCLUDING CABINET FITTINGS, SPEAKER GRILLES, CROSS-OVERS AND HIGH POWER, HIGH FREQUENCY BULLETS AND HORNS, LARGE (A4) S.A.E. (60p STAMPED) FOR COMPLETE LIST.

McKenzie and Fane Loudspeakers are also available.

EMINENCE:- INSTRUMENTS, P.A., DISCO, ETC

ALL EMINENCE UNITS 8 OHMS IMPEDANCE

8″ 100 WATT R.M.S. ME8-100 GEN. PURPOSE, LEAD GUITAR, EXCELLENT MID, DISCO.
RES. FREQ. 72Hz, FREQ. RESP. TO 4KHz, SENS 97dB. **PRICE £32.71 + £2.00 P&P**

10″ 100 WATT R.M.S. ME10-100 GUITAR, VOCAL, KEYBOARD, DISCO, EXCELLENT MID.
RES. FREQ. 71Hz, FREQ. RESP. TO 7KHz, SENS97dB. **PRICE £33.74 + £2.50 P&P**

10″ 200 WATT R.M.S. ME10-200 GUITAR, KEYB'D, DISCO, VOCAL, EXCELLENT HIGH POWER MID.
RES. FREQ. 65Hz, FREQ. RESP. TO 3.5KHz, SENS 99dB. **PRICE £43.47 + £2.50 P&P**

12″ 100 WATT R.M.S. ME12-100LE GEN. PURPOSE, LEAD GUITAR, DISCO, STAGE MONITOR.
RES.FREQ. 49Hz, FREQ. RESP. TO 6KHz, SENS 100dB. **PRICE £35.64 + £3.50 P&P**

12″ 100 WATT R.M.S. ME12-100LT (TWIN CONE) WIDE RESPONSE, P.A., VOCAL, STAGE MONITOR. RES. FREQ 42Hz, FREQ. RESP. TO 10KHz, SENS 98dB. **PRICE £36.67 + £3.50 P&P**

12″ 200 WATT R.M.S. ME12-200 GEN. PURPOSE, GUITAR, DISCO, VOCAL, EXCELLENT MID.
RES. FREQ. 58Hz, FREQ. RESP. TO 6KHz, SENS 98dB. **PRICE £46.71 + £3.50 P&P**

12″ 300 WATT R.M.S ME12-300GP HIGH POWER BASS, LEAD GUITAR, KEYBOARD, DISCO ETC.
RES. FREQ. 47Hz, FREQ. RESP. TO 5KHz, SENS 103dB. **PRICE £70.19 + £3.50 P&P**

15″ 200 WATT R.M.S. ME15-200 GEN. PURPOSE BASS, INCLUDING BASS GUITAR.
RES. FREQ. 46Hz, FREQ. RESP. TO 5KHz, SENS 99dB. **PRICE £50.72 + £4.00 P&P**

15″ 300 WATT R.M.S. ME15-300 HIGH POWER BASS, INCLUDING BASS GUITAR.
RES. FREQ. 39Hz, FREQ. RESP. TO 3KHz, SENS 103dB. **PRICE £73.34 + £4.00 P&P**

EARBENDERS:- HI-FI, STUDIO, IN-CAR, ETC

ALL EARBENDER UNITS 8 OHMS (Except EB8-50 & EB10-50 which are dual impedance tapped @ 4 & 8 ohm)

BASS, SINGLE CONE, HIGH COMPLIANCE, ROLLED SURROUND

8″ 50watt EB8-50 DUAL IMPEDENCE, TAPPED 4/8 OHM BASS, HI-FI, IN-CAR.
RES. FREQ. 40Hz, FREQ. RESP. TO 7KHz SENS 97dB. **PRICE £8.90 + £2.00 P&P**

10″ 50WATT EB10-50 DUAL IMPEDENCE, TAPPED 4/8 OHM BASS, HI-FI, IN-CAR.
RES. FREQ. 40Hz, FREQ. RESP. TO 5KHz, SENS. 99dB. **PRICE £13.65 + £2.50 P&P**

10″ 100WATT EB10-100 BASS, HI-FI, STUDIO.
RES. FREQ. 35Hz, FREQ. RESP. TO 3KHz, SENS 96dB. **PRICE £30.39 + £3.50 P&P**

12″ 100WATT EB12-100 BASS, STUDIO, HI-FI, EXCELLENT DISCO.
RES. FREQ. 26Hz, FREQ. RESP. TO 3 KHz, SENS 93dB. **PRICE £42.12 + £3.50 P&P**

FULL RANGE TWIN CONE, HIGH COMPLIANCE, ROLLED SURROUND

5¼″ 60WATT EB5-60TC (TWIN CONE) HI-FI, MULTI-ARRAY DISCO ETC.
RES. FREQ. 63Hz, FREQ. RESP. TO 20KHz, SENS 92dB. **PRICE £9.99 + £1.50 P&P**

6½″ 60WATT EB6-60TC (TWIN CONE) HI-FI, MULTI-ARRAY DISCO ETC.
RES. FREQ. 38Hz, FREQ. RESP. TO 20KHz, SENS 94dB. **PRICE £10.99 + 1.50 P&P**

8″ 60WATT EB8-60TC (TWIN CONE) HI-FI, MILTI-ARRAY DISCO ETC.
RES. FREQ. 40Hz, FREQ. RESP. TO 18KHz, SENS 89dB. **PRICE £12.99 + £1.50 P&P**

10″ 60WATT EB10-60TC (TWIN CONE) HI-FI, MULTI ARRAY DISCO ETC.
RES. FREQ. 35Hz, FREQ. RESP. TO 12KHz, SENS 98dB. **PRICE £16.49 + £2.00 P&P**

TRANSMITTER HOBBY KITS

PROVEN TRANSMITTER DESIGNS INCLUDING GLASS FIBRE PRINTED CIRCUIT BOARD AND HIGH QUALITY COMPONENTS COMPLETE WITH CIRCUIT AND INSTRUCTIONS

3W TRANSMITTER 80-108MHz, VARICAP CONTROLLED PROFESSIONAL PERFORMANCE, RANGE UP TO 3 MILES, SIZE 38 x 123mm. SUPPLY 12V @ 0.5AMP.
PRICE £14.85 + £1.00 P&P

FM MICRO TRANSMITTER 100-108MHz, VARICAP TUNED, COMPLETE WITH VERY SENS FET MIC, RANGE 100-300m, SIZE 56 x 46mm, SUPPLY 9V BATTERY.
PRICE £8.80 + £1.00 P&P

PHOTO: 3W FM TRANSMITTER

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VIEWS OF THE BRIDGE

Part 2: Instrumentation applications

By Bryan Hart

Instrument rectifiers

The diode bridge, in conjunction with a moving-coil meter, enables us to measure the peak value, U_p, of a sinusoidal signal voltage, or alternatively its root-mean-square (r.m.s.) value, $U_p/\sqrt{2}$.

Consider **Fig. 13**. The arrowed full-line sections show the path of current flow for positive-going half cycles ($i>0$), and the arrowed dotted-lines that for negative-going half cycles ($i<0$). For ideal diodes, the rectified current waveform is shown in **Fig. 14**. The meter movement can not follow rapid variations in current because of mechanical inertia. The net result is that the pointer indicates a mean value $\bar{I}$. This corresponds to that constant level of i for which the area of the hatched region above it is equal to that of the hatched region below.

$\bar{I}$ is related to U_p by the relationship

$$\bar{I} = 2U_p/\pi R = 0.636\,(U_p/R).$$

Making the design choice R = 6.36 kΩ, for easy current-scaling, gives $\bar{I}$ = 1 mA for U_p = 10 V. Alternatively, for R = 63.6 kΩ, $\bar{I}$ = 100 μA for U_p = 10 V.

R can be range-switched to suit the signal amplitude being measured.

Connected across the secondary of an isolation transformer having a turns ratio 1:1, the circuit of **Fig. 13** is capable of giving an accurate indication of mains voltage amplitude (U_p = 340 V). However, the circuit is clearly limited in the measurement of small amplitude signals because of the finite voltage drop of real diodes.

A solution to the problem of measuring voltages in the millivolt range is provided by the use of the circuit in **Fig. 15**. In this, R is made the input arm of an opamp inverter configuration that has the diode quad as the feedback network. Note that the drawing of the bridge is rotated anti-clockwise through a right angle compared with that shown in **Fig. 13**, for ease in explaining circuit operation, but the load is still connected between terminals **X** and **Y**.

The action of negative feedback forces **A** to be a 'virtual-earth' point. Hence, the whole of U_s appears across R and the conducting diodes and meter (M) are forced to pass a current, U_s/R, that is independent of the magnitude of the diode drops. **Figure 14** again applies to i and **Fig. 16** shows circuit voltage waveforms. When U_s goes positive, **A** attempts to rise but the amplifier output switches sufficiently negative (approx. –1.4 V) for D_2, D_4 to conduct the current i (= U_s/R) necessary to keep **A** at earth potential. Similarly, U_0 switches to 1.4 V when U_s goes negative. An upper limit to signal frequency is set by the slew rate of the operational amplifier, because it determines the time taken for U_0 to switch from –1.4 V to +1.4 V and vice versa. The popular 741 operational amplifier is acceptable for signals in the low kilohertz range.

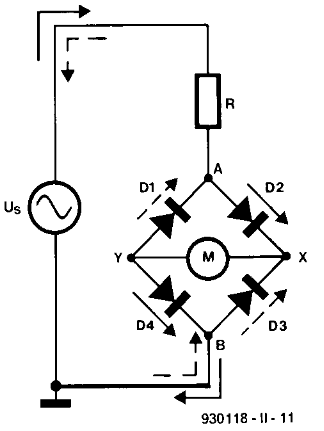

Fig. 13. Basic instrument rectifier. Arrowed full lines are for $i > 0$; dashed lines for $i < 0$.

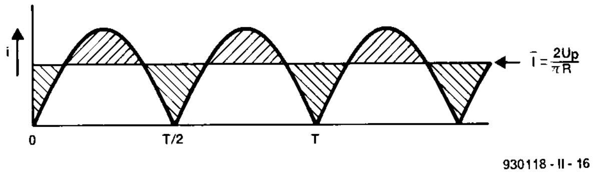

Fig. 14. Idealized current waveform for Fig. 13.

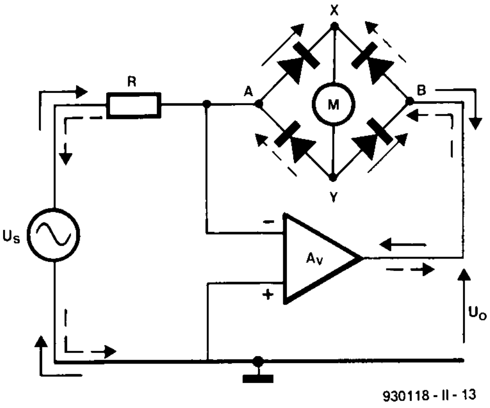

Fig. 15. Precision instrument rectifier.

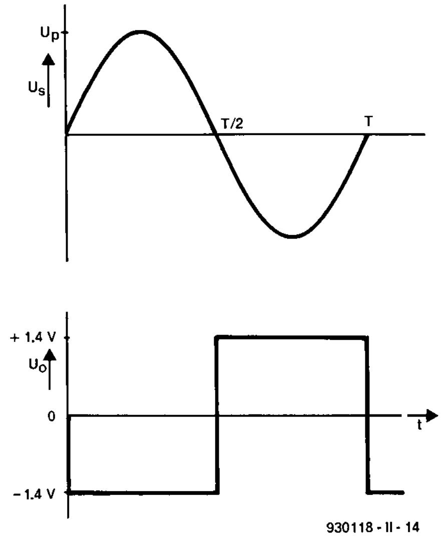

Fig. 16. Voltage waveforms for Fig. 15.

The input resistance of the circuit of **Fig. 15** is R. To minimize loading of a circuit being monitored, the alternative high input-impedance circuit of **Fig. 17** can be used. The opamp now operates in the non-inverting mode. By 'follower' action $U_A = U_s$ so the current forced through M is U_s/R. Once again, **Fig. 14** shows the time variation of this current and its mean value.

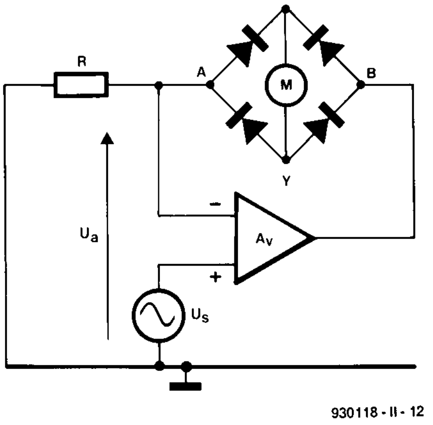

Fig. 17. Instrument rectifier with high input impedance.

The diode-bridge gate

The diode bridge, usually with a pair of additional gating diodes, makes a versatile switch for generating and processing waveforms.

Figure 18 shows a basic arrangement. In this application, the bridge of **Fig. 13** is rotated clockwise through a right angle. Also, the input is now at **B** and the output at **A**. Control waveforms for switching the bridge on and off are applied to terminals **Y** and **X** via gating diodes D_5, D_6.

The constant-bias currents, I_0, can be the outputs of current-mirrors or grounded-base stages. The operational amplifier, strapped as a unity-gain voltage-follower, provides a buffered output so that impedance Z is not

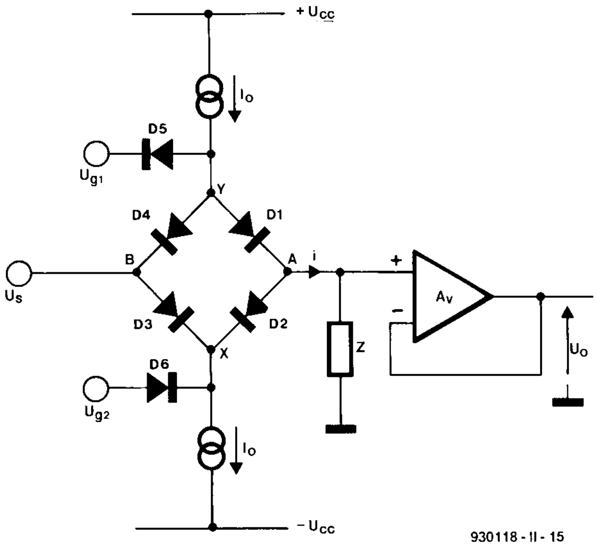

Fig. 18. Diode bridge gate.

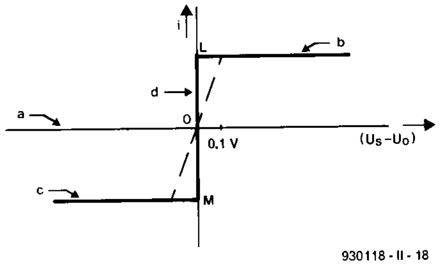

Fig. 19. An idealized *i* vs ($u_S - u_C$) plot, with lettered conduction states, for Fig. 18. Dashed line shows actual characteristic d.

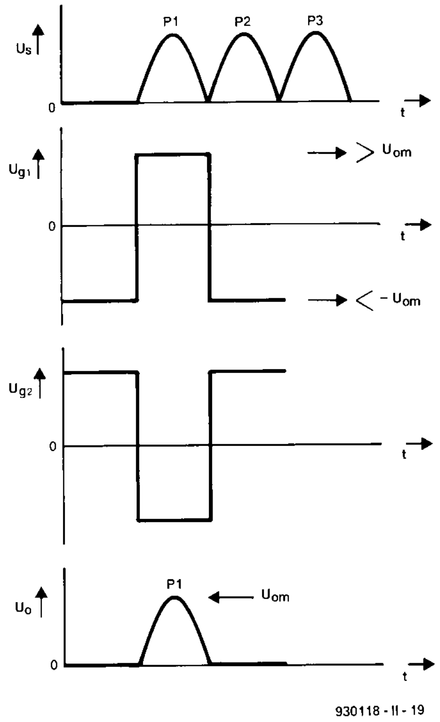

Fig. 20. Analogue gate waveforms.

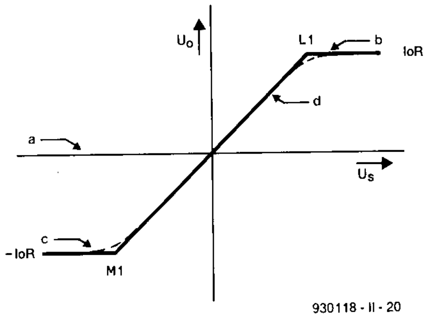

Fig. 21. Transfer characteristics of analogue gate.

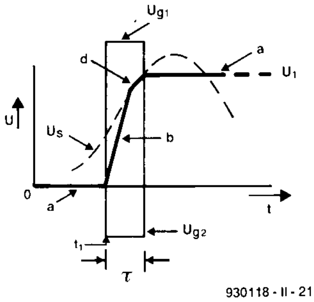

Fig. 22. Operation of sample-and-hold (S/H) gate.

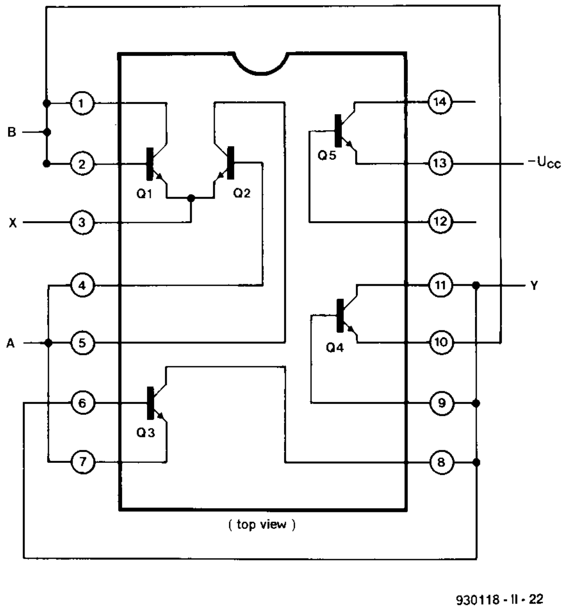

Fig. 23. Bridge with matched ‘diodes’ using IC array Type 3046.

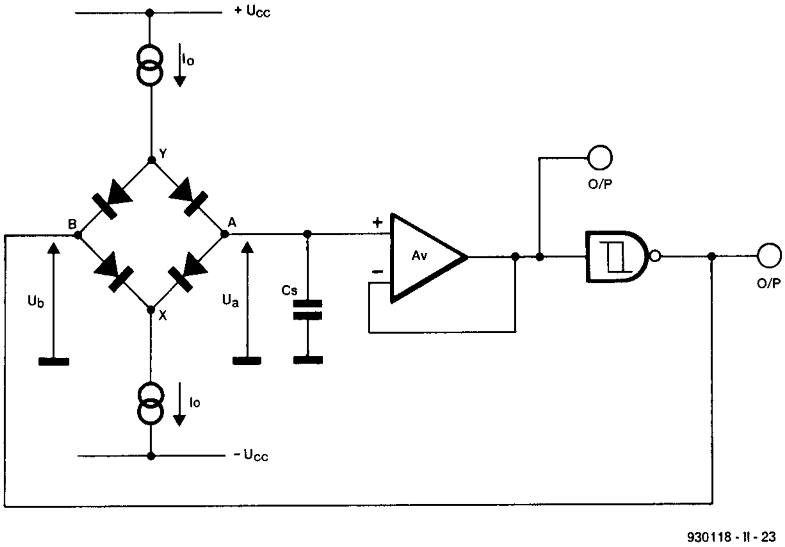

Fig. 24. Symmetrical triangle voltage generator using a bridge. Note that D_5 and D_6 are not necessary here.

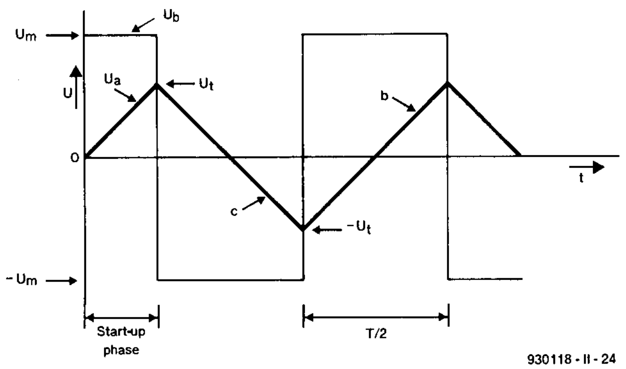

Fig. 25. Waveforms for Fig. 23 with lettered diode conduction states. The 'start-up' phase is not observed on an oscilloscope trace.

	Diode Condition ●					
Mode	D1	D2	D3	D4	D5	D6
a					●	●
b	●		●			
c		●		●		
d	●	●	●	●		

● Dot indicates diode on

930118 - II - 17

Table 1. Operating mode and diode conduction states for Fig. 18.

loaded.

Possible operating modes *a, b, c, d,* that are related to the conducting states of the diodes, are shown in **Table 1**. The characteristic relating the current *i* in *Z* to the differential voltage ($U_S - U_0$) is shown, correspondingly labelled, in **Fig. 19**.

For *a*, the 'off' state, U_{G1} and U_{G2} of **Fig. 15** have the polarity and amplitude required to hold the bridge diodes reverse-biased for the maximum U_S, so $U_0 = 0$. Hence, the characteristic is the axis of ($U_S - U_0$).

In the 'on' state, the idealized characteristic of **Fig. 19** comprises the three straight line sections. Departure from the ideal, when real diodes are used, is indicated by the dotted line.

There are two basic gate applications of the bridge: the 'linear', 'analogue' or 'transmission' gate for which *Z*, in **Fig. 18**, is a resistor, *R*, and a sample-and-hold (S/H) gate in which case *Z* is a capacitor, C_S.

Consider, first, the linear gate. The waveforms of **Fig. 20** illustrate a typical application in the field of nuclear instrumentation. A pulse, P_1, from a particle detector is time-selected from a series of such pulses so that its shape and amplitude can be examined in detail.

The relevant transfer characteristic (**Fig. 21**) is derived from **Fig. 19**; thus, points L_1, M_1 of **Fig. 21** correspond, respectively, to *L*, *M*, of **Fig. 19**. For the output to be an acceptable copy of the input when the gate is on, it is necessary to operate on section **d** (**Fig. 21**) only. Furthermore, if the magnitude of the maximum output voltage required is U_{om}, then, to minimize distortion, it is desirable that

$$I_0 R \geq 10 U_{om}.$$

Thus, for $U_{om} = 1$ V, $I_0 R \geq 10$ V. This does not fix the individual values of I_0 and *R* and it might seem that the choice I_0 = 2 mA, *R* = 5 kΩ, would be as good as an alternative such as I_0 = 10 mA, *R* = 1 kΩ.

However, the second choice would often be preferable because it offers faster operation. More current is available to charge unavoidable circuit stray capacitances (not shown) when the gate switches from the off to the on state and vice versa. A greater speed potentiality is what makes the diode bridge superior to currently available CMOS transmission gates (e.g., 4016 range).

Consider, next, an S/H gate. One of its many uses is with an analogue-to-digital converter (ADC) when a speech signal is to be transmitted digitally over a link.

Figure 22 shows what happens when the bridge is switched on at t_1 by a sampling pulse of duration τ. *Z* is now a capacitor, C_S, which charges up to U_1. This is stored until a further sample is taken because there is (ideally) no discharge path when the gate is switched off. During the 'hold' phase there is adequate time for an ADC to digitize U_1. In the worst case, C_S may be required to charge from its maximum permitted negative value $-U_{om}$ to its maximum allowable positive value U_{om}, and this requires a charge $2C_S U_{om}$. As the charge available in the interval τ is $I_0 \tau$, this leads to the condition

$$I_0 \tau \geq 2 C_S U_{om}.$$

A second condition involves the amplifier slew rate, *S* (V µs^{-1}). If I_0 is expressed in mA and C_S in nF, then we require $S > I_0 / C_S$ so that the amplifier output can follow the charge and discharge of C_S. Suppose, for example, that I_0 = 10 mA and C_S = 1 nF. Then, *S*>(10 V µs^{-1}). This means the use of an FET operational amplifier such as the 351. FET opamps also have a very low input current so capacitor discharge in the 'hold' state is minimized.

For optimum circuit performance, the linear gate and the S/H gate should both employ bridges in which the diodes are matched in their respective static and dynamic parameters. Matching by selection is a tedious and costly procedure. Fortunately, there is a way of avoiding it that may be applicable in some cases. It entails using a matched IC transistor array with the transistors strapped as diodes. **Figure 23** shows the connection pattern for the popular, low-cost CA3046 array.

As a final instrumentation application of the bridge, consider the waveform generator outlined in **Fig. 24**. The bridge, a buffer amplifier and a Schmitt trigger are connected together in a loop. Diodes D_5 and D_6 are not required in this circuit.

The Schmitt has trigger levels of $\pm U_T$ and it swings between the limits $\pm U_M$. Circuit waveforms, lettered according to the diode conduction state of **Table 1**, are shown in **Fig. 25**. The capacitor charges and is discharged at a constant rate, set by I_0, during a time interval $T/2$. The change in charge is $2C_sU_T$ and this must be equal to $I_0T/2$. If we write f_p (pulse repetition frequency) = $1/T$, then

$$f_p = I_0/4C_sU_T.$$

Regarding I_0 as a variable, under the control of an external input signal, leads to the idea of a current-controlled oscillator. Using a voltage-to-current converter, we obtain a voltage-controlled oscillator, which is important in signal transmission and phase-locked loops. END

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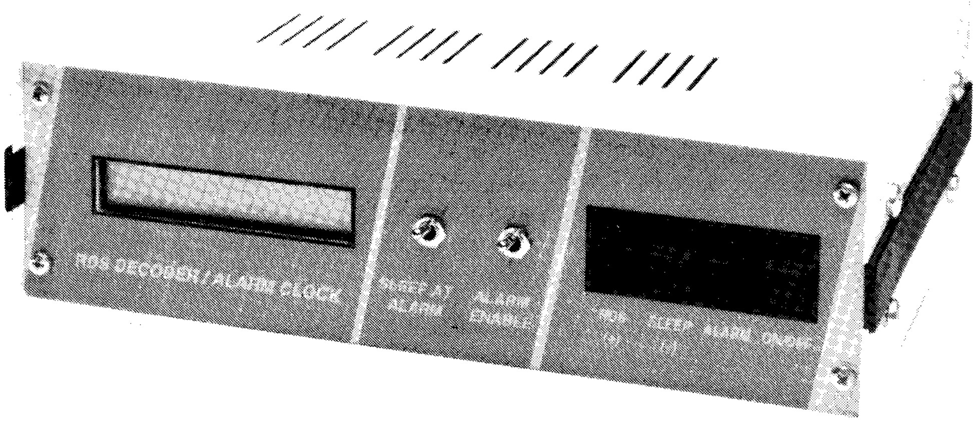
RADIO DATA SYSTEM (RDS) DECODER WITH CLOCK/ALARM FUNCTION

This article describes a compact radio data system (RDS) decoder based on two extremely powerful, yet affordable, ICs, the Philips Components SAA6579T RDS demodulator and the Motorola MC68HC05E0 microprocessor.



By Peter Topping

THE Radio Data System (RDS) adds digital data capability to the VHF FM broadcasts on band III (87.5 to 108 MHz), and is in use in most of Western Europe. The specification is defined in EBU technical document number 3244 (see Ref. 1). A description of the capabilities of RDS can be found in previous *Elektor Electronics* articles (Refs. 2 and 3), but a brief recap is given here.

To transmit the data, a subcarrier is added at 57 kHz, three times the stereo pilot tone. This subcarrier is amplitude-modulated with a bi-phase coded signal. The subcarrier itself is suppressed to avoid data-modulated cross-talk in phase-locked loop stereo decoders, and to maintain compatibility with the German ARI (Autofahrer Rundfunk Information) system, which uses the same subcarrier frequency. Information is sent in groups of four 26-bit blocks. Each group of 104 bits is one of several types containing different information. It is up to the broadcaster which features are transmitted as long as the specified format is adhered to, and PI, PTY and TP are included. Each group contains a different sub-set of the RDS features. A list of all currently defined RDS features is shown in **Table 1**.

The retrieval of data is carried out by demodulation hardware which generates clock and data signals that can be used by a microprocessor. Suitable devices that can perform this function include the SAF7579T, SAA6579, TDA7330 and LA2231. The *Elektor Electronics* RDS demodulator board (Ref. 2) is based on the SAF7579T. The SAA6579 used in the present decoder is a similar device that integrates the filtering, and thus requires fewer external components (Ref. 4). Those of you who have already built the SAF7579T-based demodulator will be pleased to know that this unit may be linked to the present decoder via connector K_1.

The block diagram of the RDS decoder is shown in **Fig. 1**. The MPX (multiplex) signal needed to drive the RDS decoder is 'tapped' from the FM tuner. In most cases, it can be found straight after the FM demodulator, i.e., ahead of the stereo decoder and/or any low-pass filter(s) that may be fitted.

The microprocessor, in this case a Motorola MC68HC05E0, decodes the RDS data using the clock and data signals from the demodulator, and sends selected data to a dot-matrix module, which can be an LCD or a vacuum fluorescence type.

The decoder incorporates an alarm clock which, if permanently powered, can be used to switch on the radio supplying the RDS data at the required alarm time.This is achieved with the aid of a relay contact on connector K_4. The relay contact could control the power supply of the radio, or only the audio stage. If an audio mute is used, RDS data can be updated even when the radio is 'off'. The radio is then always switched on at the right time, even when a change from summer to winter time (or vice versa) has occurred. Alternatively, the decoder can be used to simply display RDS data with its power being supplied from the radio, and manually switched on and off.

There is a second output intended

MAIN SPECIFICATIONS

- Permanent display of PS name and time or date and time (depending on mode).
- Optional display of PI code and secondary RDS features (RT, PTY, PIN, MS, DI, TA, TP, MJD and EON) on demand, including the principal frequencies of up to 11 other networks.
- Full use of CT providing auto-setting, accurate clock with automatic date and summertime adjustment.
- Implemented as an alarm clock which can control the power to the radio and/or sound an alarm.
- Sleep timer.
- TA=TP=1 (traffic announcement taking place) output.

R·D·S RADIO DATA SYSTEM

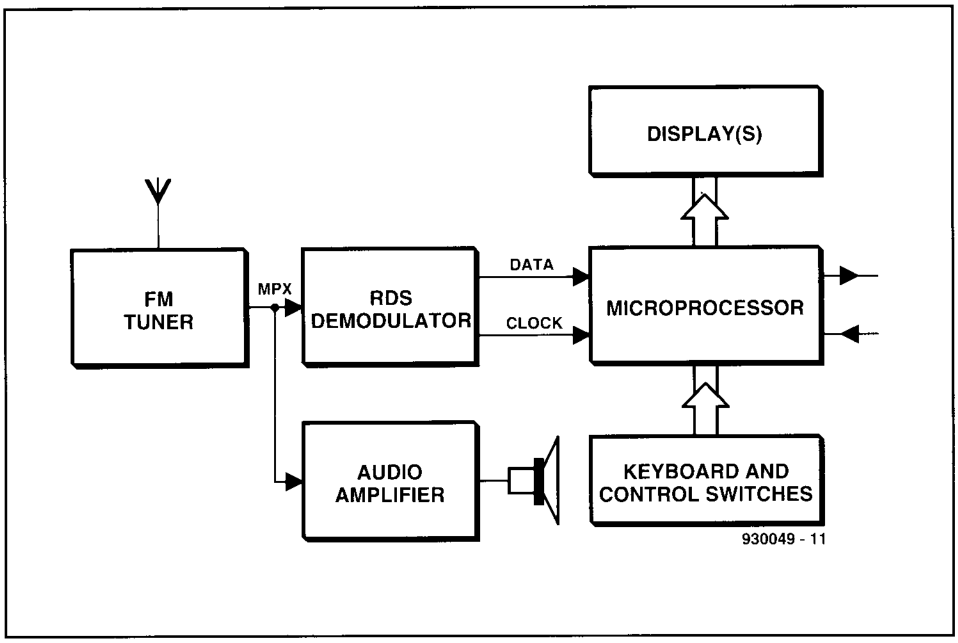


Fig. 1. Block diagram of the RDS decoder.

Feature	Information
PI	Program identification
PTY	Program type
PS	Program service name
RT	Radiotext
CT	Clock time and date
AF	Alternative frequencies
TA	Traffic announcement
TP	Traffic program
MS	Music/speech switch
DI	Decoder identification
PIN	Programme item number
EON	Enhanced other networks
TDC	Transparent data channel
INH	In-house data

Table 1. RDS features.

PTY	Display
0	no programme type
1	News
2	Current affairs
3	Information
4	Sport
5	Education
6	Drama
7	Culture
8	Science
9	Varied
10	Pop music
11	Rock music
12	Easy listening
13	Light classics
14	Serious classics
15	Other music
16-31	No programme type

Table 2. PTY types.

to sound a beeper. This output is cancelled when any key is pressed, leaving the control output active.

RDS features supported

The present decoder supports PI, PTY, PS, RT, CT, TP, TA, MS, DI, PIN and EON. It facilitates permanent display of the 8-digit station name (PS) and time (CT) and, on request, can display program type (PTY), radiotext data (RT) and the status of the other RDS features. EON data can be displayed, but the retuning features associated with AF and EON are not supported as there is no capability to control the tuned frequency. In a car radio, EON data is used to switch the radio to a station which is broadcasting local traffic information, while AF data is used to tune the radio to the strongest signal carrying the selected device.

Program identification (PI) is a two-byte number which identifies the country, coverage area and service. It can be used by the control microprocessor, but is normally intended for display. A change in PI code causes the initialization of all RDS data as it indicates that the radio has been detuned. This decoder facilitates the display of the current PI code on request.

Program type (PTY) is a 5-bit number which indicates the type of program being broadcast. At present, 16 of these types are defined. Examples include 'no programme type', 'current affairs' and 'pop music', although the actual syntax which is displayed is determined by the software of the controlling microprocessor. In this example, PTY can be displayed on request — **Table 2** shows the display used for each PTY code.

Program Service Name (PS) is the eight character name of the station, and is permanently displayed (except in standby mode).

Radiotext (RT) constitutes a string of up to 64 characters which give additional information regarding the service or programme being transmitted. In this application, RT is displayed on request on the 16-digit dot matrix using scrolling. The data often contains extra spaces to centre the text on a 2×32 character display. As these are not appropriate for a 16-character scrolling display, the software reduces all sequences of two or more spaces to a single space.

Clock Time (CT) data is transmitted every minute on the minute, and provides a very accurate clock, traceable to national standards. The (modified Julian) date and local time variation is also transmitted. Time is permanently displayed. In standby mode (see below), the date is displayed instead of the PS name. The MJD number, which is the form in which the date is transmitted, can also be displayed. The microprocessor converts this number into day-of-week, day-of-month, month-of-year.

Alternative Frequencies (AF) would be used by a car radio to retune to the strongest signal carrying the selected service. AF data, along with TDC and INH, is not used in this application.

Traffic Announcement (TA) and Traffic program (TP) are flags. TP is set if the transmitter normally carries traffic information, and TA is set if a traffic announcement is in progress. The combination TA=1 and TP=0 is used to indicate that EON data is being used to supply information to other networks, including traffic announcements. The status of these flags can be displayed, and the combination TA=TP=1 is brought out to microcontroller pin 68, and is used to control an LED or external hardware, which could demute the radio, or switch from cassette when a traffic announcement is taking place.

Music-Speech (MS) is a single bit indicating either music or speech, and is intended to be used to make a tone or volume adjustment to a radio's audio stage. The MS bit is displayed on request.

Decoder Information (DI) constitutes four bits indicating the type of transmission (mono, stereo, binaural, etc.). It is not essentially in use in the UK, but can be displayed as a number be-

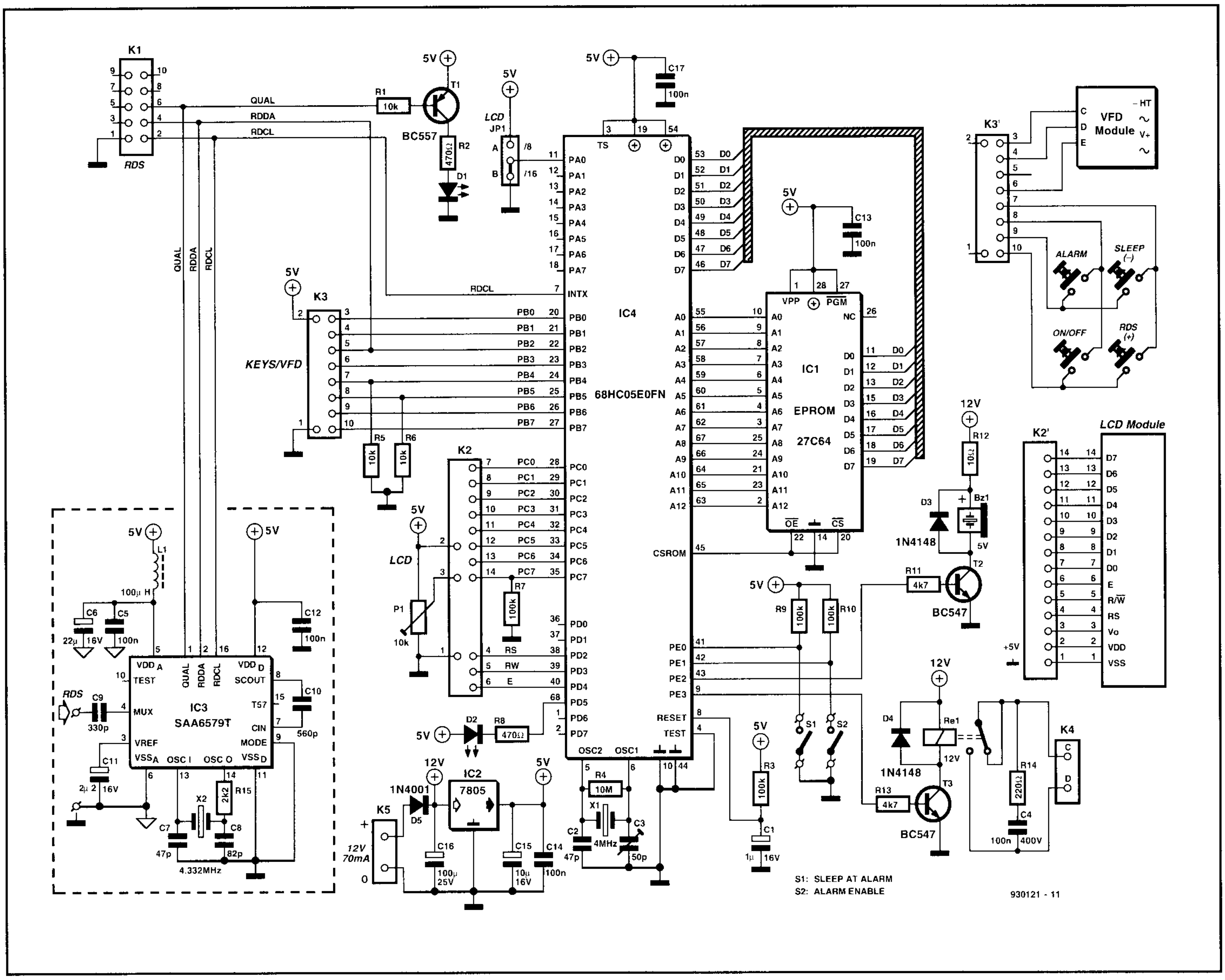


Fig. 2. Circuit diagram of the RDS decoder.

tween 0 and 15.

Programme Item Number (PIN) is used to identify the programme currently being broadcast. The format is a 2-byte number which includes the scheduled time and date (day-of-month) of the start of the programme. It can be displayed as four hexadecimal digits, or fully decoded to day-of-month and time. Once it is fully implemented, PIN information will be able to facilitate automatic switch-on or recording of a pre-selected programme when it actually starts, even if this is not at the scheduled time.

Enhanced Other Networks (EON) replaces the older Other Network (ON) format. If type-14 groups are used to provide EON data, then type-3 groups (ON) will not be used (**Table 5** shows the currently defined group types). Type-14A groups are used to send information about other networks. The PS name and principal frequency of up to 11 other networks can be displayed on request. Type-14B groups are used to switch to traffic announcements on other stations in a radio in which the microprocessor can control the tuned frequency.

Circuit description

Figure 2 shows the circuit diagram. An external RDS demodulator, if used, may be connected to K_1, when the circuit around IC_3 is, obviously, omitted. Here, it is assumed that you use the SAA6579T from Philips Compo-nents, which is accommodated on the board. Only a handful of passive parts, including a 4.332 MHz quartz crystal, are needed to get going with the SAA6579T, of which the block diagram is shown in **Fig. 3**. The demodulated, but unfiltered, MPX signal is applied to the demodulator via the MUX input pin. This signal has a bandwidth of about 60 kHz, and is supplied by the FM radio. As regards the bandwidth, it is essential that the MPX signal arrives unfiltered, i.e., it must contain the 57-kHz component which carries the RDS information. No filtering of any kind is allowed on this signal, so be sure to find the right point to 'tap' in your FM radio.

A remarkable feature of the SAA6579T is that it has an on-chip eighth-order 57-kHz bandpass filter with a bandwidth of only 3 kHz. The IC automatically regenerates the 57-kHz subcarrier, and extracts the RDS data with the aid of a synchronous modulator. After some more processing, the data and clock signals that belong with the RDS signal are output via pins RDDA and RDCL respectively. The microprocessor uses these two signals to decode the actual information conveyed via the radio. A thirs signal, QUAL, is used to mark good (QUAL=high) or bad (QUAL=low) reception of RDS data. The processor does not use this signal. However, a LED (D_1) lights when reception is too poor to warrant valid RDS data.

The circuit of the decoder is very simple as the MC68HC05E0 uses a non-multiplexed bus, and includes its own chip selects. The only other chip required is an 8-KByte 27C64 EPROM

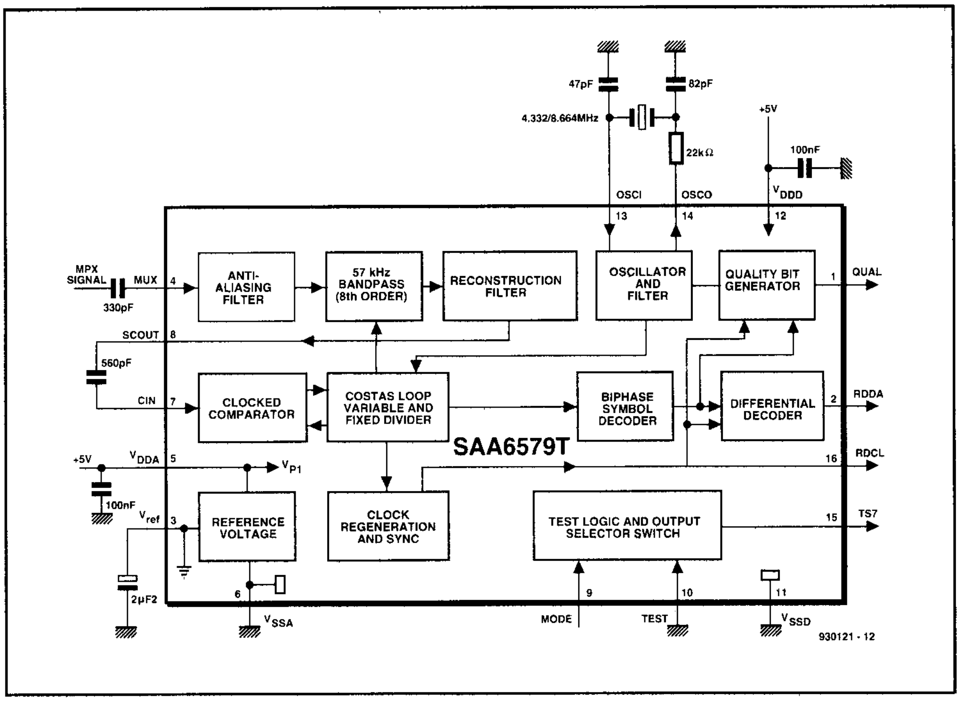


Fig. 3. Internal diagram and typical external parts connection of SAA6579T (courtesy Philips Components).

MODE	KEY			
	On/Off	Sleep	Alarm	RDS
Standby (Off)	mode normal (On)	mode sleep (On)	mode alarm	—
Normal (On)	mode stndby (Off)			RT PTY PI TA/TP PIN(h) PIN(d) MJD MS/DI EON 1 : : EON 11
Alarm OFF			mode alarm ON	
Alarm ON	mode alarm set-up		mode alarm OFF	
Alarm SET UP	toggle hr/min	dec. hr/min		inc. hr/min

Table 3. Key functions.

Display mode		Format
Standby (Off)	Alarm off	Thu 30 Apr 18:05
	Alarm off, no CT	Mon 0 inv 0:00
	Alarm on	0659 ALARM 18:05
Normal (On)	With RDS PS name	BBC R4 18:05
	Without RDS	-------- 18:05
Alarm	Alarm off	Alarm - OFF
	Alarm on	Alarm - 6:59
Sleep		Sleep 60 min.
RDS	RT	BBC Radio 4 ....
	PTY	News
	PI	PI code - C204
	TA & TP	TP - 0 TA - 1
	PIN(hex)	PIN no. - F480
	PIN(decod)	30th at 18:00
	MJD	MJ day - 48742
	MS & DI	M/S M DI 15
	EON 1	BBC R3 92.10
	2	BBC R.Sc 103.60
	3	BBC Nwcl 96.00
	4	BBC Scot 94.30
	5	BBC Mtme 92.50
	6	BBC Twed 93.50
	7	.BBC R5 909kHz
	8	BBC Eng. 100.00
	9	BBC R1 99.50
	10	BBC R2 89.90
	11	--------

Table 4. Display formats.

of which about 4½ K is used. The EPROM is available ready-programmed through our Readers Services (see p. 70).

In order to facilitate a choice of display technology, the decoder is capable of driving both a parallel LCD module (based on a HD44780 controller, with or without an HD44100 driver) and a serial VFD module (based on an MSC7128 driver). The displays show the same data (within the limitations of their character ROMs). Either or both modules can be connected — the choice is up to you.

LCD modules using only the HD44780 use divide-by-16 multiplexing. The software is written for this type of display, and will also work with modules incorporating the additional HD44100. Modules with both chips are capable of higher contrast, by employing divide-by-8 multiplexing. To use this capability, fit jumper JP$_1$ as required: position 'A' for ÷8 multiplexing, for which a HD44100 must be present in the LCD module; or position 'B' for 1÷16 multiplexing (no HD44100 fitted).

It is also possible to connect a serially driven VFD module, which shows the same data as the LCD module. The display driver used has a different character set from the standard ASCII set used by the LCD module, and a table is used to convert ASCII data into the required characters on the VFD module. If a VFD module is connected, R$_7$ should be connected to bit 7 of port C. This bit is read by the microprocessor to check that the controller in the module is ready to receive a command, and may cause the software to hang up if it is left open-circuit.

The only other components required are a crystal, the 4-key keyboard, two switches, and a few passive components. Correct operation of the clock in the absence of an RDS signal requires that a 4.000-MHz crystal be used (trimmer C$_3$ on pin 6 should be adjusted for accurate timekeeping).

Principle of operation

On power-up, the software initializes the display modules (the display shows '- - - - - 00:00' until a valid group 4A is received) and an idle loop regularly checks the local keyboard for a key press, compares the current time with the alarm time, and performs other time-dependent functions related to the display modules and the sleep timer.

The keyboard software scans the 4-key matrix for a key press every 16 ms. If the same key is pressed on three successive scans, it acts on this key function by calling the relevant subroutine. These routines also control the repeat rate of the SLEEP and RDS keys. This rate is set at 6 Hz (after an initial 750-ms delay) when the keys are used to change the alarm time, and 1 Hz for their normal function. The other keys do not repeat if held down. **Table 3** shows the various functions available in each mode.

The **On/Off key** toggles between ON and standby modes. A port pin (3, Port E) can be used to control the power to the VHF radio and/or other external hardware. It is active high (low in

RADIO DATA SYSTEM GROUP FEATURES

Groups handled

If a complete group has been received, the data can be processed. The PI code is checked to see if it has changed. If it has, the displays are initialized. In an application using the AF capability of RDS, more use would be made of the PI code. All RDS data, except date and time, is cleared if no valid RDS data is detected for a period of 10-seconds.

Next, PTY and TP are updated, and the group type identified. Group types 0A, 0B, 1A, 1B, 2A, 4A, 14A and 15B are handled. Table 6 shows the type of information contained in each group, and Table 7 shows the detailed structure of these groups.

Groups 0 and 15B

As AF data is not handled, there is no difference in the treatment of groups 0A and 0B. PS data is extracted and placed in RAM according to the address bits in block 2 (see Table 6). TA, DI and MS data are then read, DI is sent a single bit at a time and uses the same address bits as the PS name to determine which of the four bits is being updated. Groups of type 15B also contain all this switching information. They are used to increase the repetition rate of this data, but contain no PS or AF information.

Group 1

Group types 1A and 1B are again treated identically as they contain the same data except for the repetition of the PI code in type 1B. The PIN data is recovered and saved in RAM.

At present the decoder simply allows the display of PIN data both in its raw hexadecimal form, and fully decoded to day-of-month and time. Full use of PIN data would require continuously comparing the PIN day-of-month and time with the current day-of-month and time, and switching on external hardware (radio and/or cassette recorder) when there is a match.

Group 2A

RT data from blocks 3 and 4 is written to RAM according to the address included in block 2. There are four address bits and four ASCII encoded bytes, giving the possibility of 64 characters. If the Text A/B flag changes state, the RT area in RAM is cleared as this indicates that the message has changed. Group 2B is not handled as it is rarely if ever used.

Group 4A

Two of the more complex tasks to be performed are required by the CT calculations for group 4A. These are for the local time difference, and the conversion of the MJD number into a recognizable date.

The broadcast time is Universal Coordinated Time (UTC, effectively the same as GMT). Time differences from UTC, including summer (daylight saving) time, are sent as an offset of up to ±12 hours in half-hour increments.

The software includes 4-function 9-digit integral BCD arithmetic which is used to decode the date from the MJD number using the formulae:

$$Y' = \mathrm{int}\,[(MJD\text{-}15078.2) / 365.25]$$

$$M' = \mathrm{int}\,[(MJD\text{-}14956.1\text{-}\mathrm{int}\{Y'\times 365.25\}) / 30.6001]$$

$$\begin{aligned} Day = {} & MJD-14956-\mathrm{int}(Y'\times 365.25)- \\ & \mathrm{int}(M'\times 30.6001) \end{aligned}$$

If $M'=14$ or $M'=15$ then $K=1$; else $K=0$

$Year = Y'+K$

$Month = M'-1-12K$

Group	Features
All	PI, PTY, TP
0	TA, DI, MS, PS, AF
1	PIN
2	RT
3	ON (replaced by EON)
4A	CT
5	TDC
6	INH
14	EON
15B	TA, DI, MS

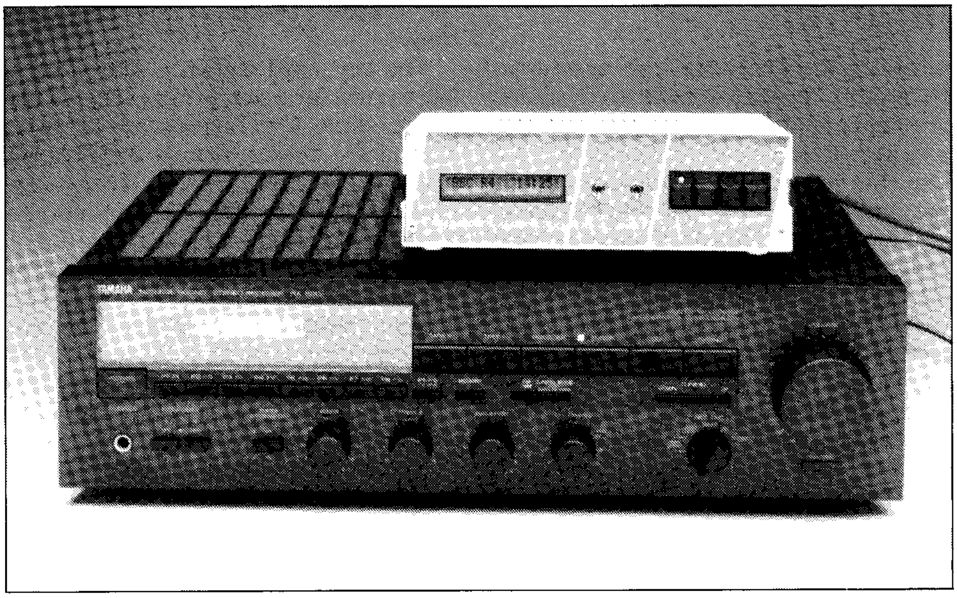
Table 5. RDS groups

Group 14A

This group contains EON data. A large amount of information can be sent using this group, and it can take up to two minutes for all the data to arrive after the radio has been retuned. This application saves the PI code, PS name and principal frequency of up to 11 networks, although more networks, each with many frequencies, and other data (e.g., PTY(ON), PIN(ON), TA(ON), etc., may be sent. Table 4 shows the format of the EON display. All the information shown in Table 4 is real data from the Black Hill transmitter in Central Scotland.

	Block 1		Block 2		Block 3		Block 4	
			bit(s) use					
Group 0 and 15B	PI code	chck A	15–12 : group no. 11 : group type 10 : TP flag 9–5 : PTY code 4 : TA flag 3 : M/S bit 2 : DI bit 1–0 : PS/DI address	chck B	AF (PI code in type 0B and 15B)	chck C or C'	PS name (as block 2 for 15B)	chck D
Group 1	PI code	chck A	15–12 : 0001 11 : group type 10 : TP flag 9–5 : PTY code 4–0 : not used	chck B	not used (PI code in type 1B)	chck C or C'	PIN data 15–11 : day-of-month 10–6 : hour 5–0 : minute	chck D
Group 2A	PI code	chck A	15–12 : 0010 11 : 0 10 : TP flag 9–5 : PTY code 4 : text A/B flag 3–0 : text address	chck B	RT 2 ASCII characters	chck C	RT 2 ASCII characters	chck D
Group 4A	PI code	chck A	15–12 : 0100 11 : 0 10 : TP flag 9–5 : PTY code 4–2 : not used 1–0 : MJD (16–15)	chck B	CT 15–1 : MJD (14–0) 0 : hour (4)	chck C	CT 15–12 : hour (3–0) 11–6 : minute (5–0). 5 : offset sense 4–0 : offset (4–0)	chck D
Group 14A	PI code	chck A	15–12 : 1110 11 : 0 10 : TP flag 9–5 : PTY code 4 : TP (On) flag 3–0 : usage code	chck B	EON information code: 0–3 : PS 4 : AF 5–9 : AF (map) 10–11 : not used 12–15 . not imp.	chck C	PI (On)	chck D

Table 6. Detailed structure of RDS groups handled.



stand-by). In stand-by mode, with the alarm disabled, the time and date are displayed. If the alarm is enabled, the alarm time is displayed along with the current RDS PS-name. **Table 4** shows these display formats.

The **Alarm key** enables the current alarm status to be displayed. A second press changes the alarm armed status. When armed, the alarm time is displayed. In this mode, the On/Off key can be used to select either hours or minutes (indicated by flashing), and the Sleep and RDS keys to increase and decrease the settings. If the alarm has triggered, the first press of any key cancels it. The alarm display has one of the two alarm formats shown in **Table 4**, according to whether or not the alarm is armed. As all the keys have a special function in the alarm

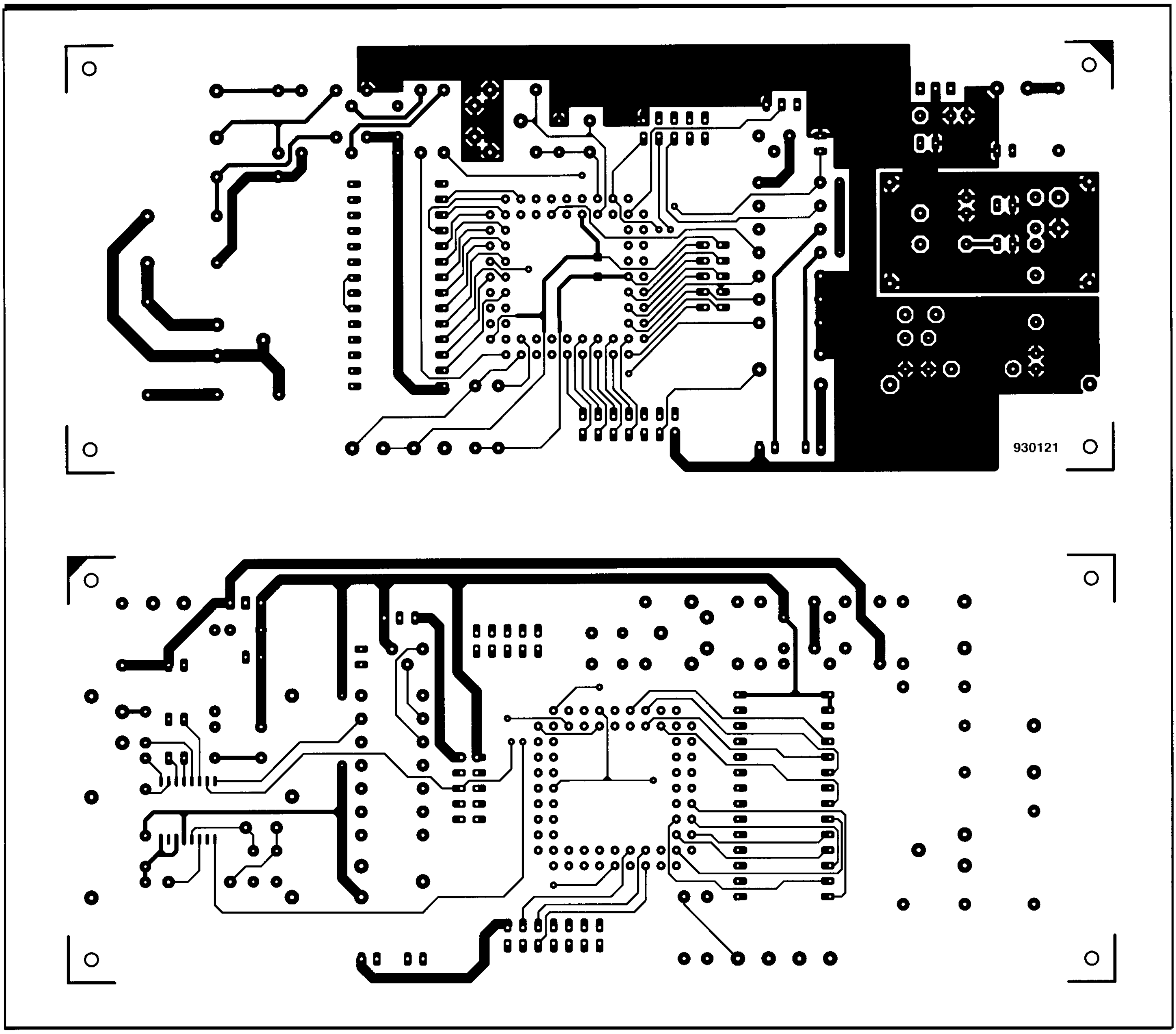


Fig. 4a. PCB component side and solder side copper layouts (direct reading).

set-up mode, the only way to exit this mode is to wait for a time-out. If no keys are pressed for five seconds, the mode returns to normal.

The **Sleep key** controls the sleep timer. If the decoder is in the standby mode, the first press of SLEEP switches it on, and initializes the sleep time to 60 minutes. Subsequent presses of the SLEEP key decrease the time remaining by 5 minutes. When the sleep timer is running, this is indicated by a flashing decimal point in the right-most character of the display modules. When the sleep time has elapsed, the decoder returns to standby. In the alarm set-up mode, this key decreases the alarm time.

The **RDS key** steps through the various RDS data displays. Holding down this key steps through the displays at 1 Hz. The displays are RT (scrolling), PTY, PI, TA/TP, PIN (hex), PIN (decoded), MJD, MS/DI and EON (11 networks) as shown in **Table 4**. In the alarm set-up mode, this key increments the alarm time.

Alarm functions

The alarm time can be entered as described above. If the alarm is enabled (alarm time displayed on the first press of the ALARM key, and permanently displayed in stand-by mode) then, at the alarm time, the auxiliary control line, PE3, will go high. This can be used to control external hardware, for example, to switch on the VHF radio supplying the RDS data, via Re_1. If the auxiliary line is already high (decoder fully on, or on via the sleep timer), then it stays high. The operation of the sleep timer is not affected if bit 0 of Port E (controlled by switch S_1) is high. If this I/O line is low at the alarm time, the sleep timer is actuated for an hour. This takes place whether the decoder was previously on, off, or running the sleep timer, and has the effect of switching the auxiliary line low an hour after the alarm time, regardless of its condition prior to the alarm.

At the alarm time, the alarm output (PE2) will also be actuated (active high) as long as it is enabled by bit 1 of port E being held low (switch S_2; alarm enable). This output is intended to drive an alarm sounder. When this output is active, a press of any key cancels it until the next alarm. This cancellation does not affect the auxiliary output.

Construction and adjustment

The artwork of the double-sided through-plated printed circuit board designed for the RDS decoder is shown in **Fig. 4**. All components are accommodated on this board, with the exception of the switches, the two LEDs and

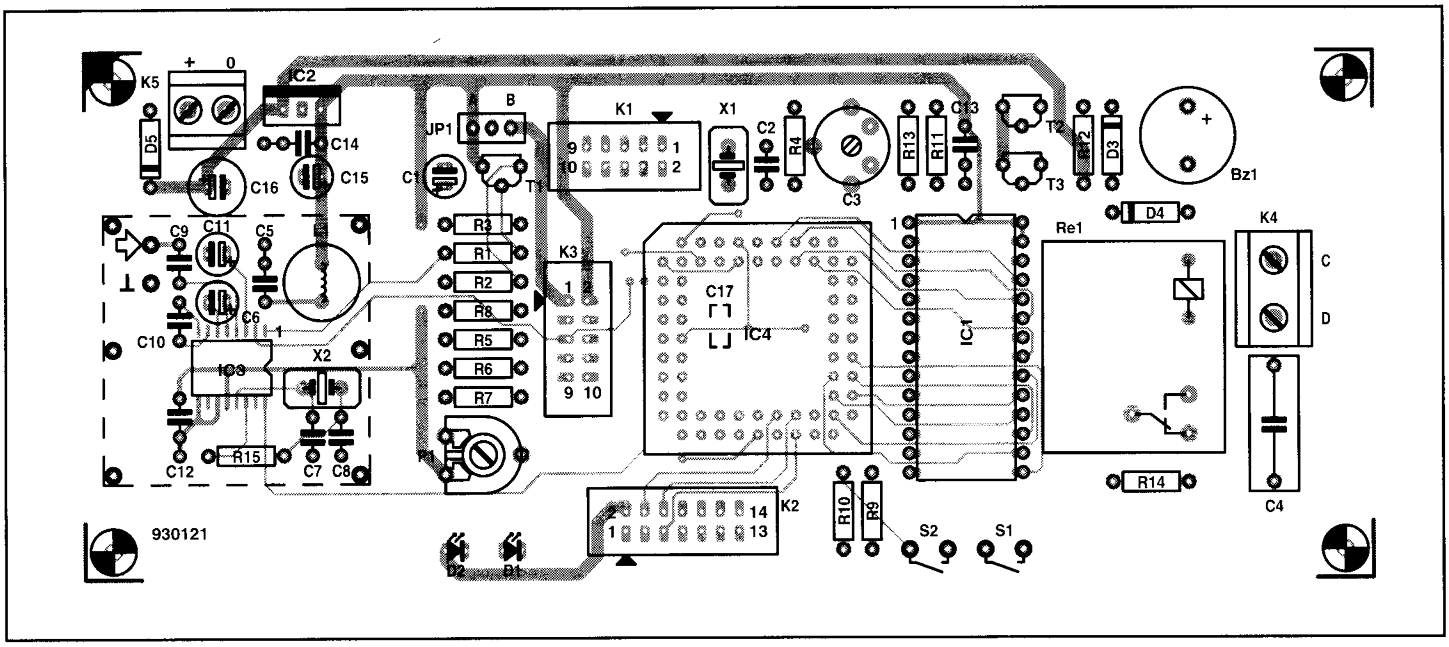


Fig. 4b. Component mounting plan.

COMPONENTS LIST

Resistors:
R1;R5;R6 = 10kΩ
R2;R8 = 470Ω
R3;R7;R9;R10 = 100kΩ
R4 = 10MΩ
R11;R13 = 4kΩ7
R12 = 10Ω
R14 = 220Ω/350V (e.g.; MRS25)
R15 = 2kΩ2
P1 = 10kΩ preset H

Capacitors:
C1 = 1µF/16V radial
C2;C7 = 47pF
C3 = 50pF trimmer
C4 = 100nF/400V
C5;C12;C13;C14 = 100nF
C6 = 22µF/16V radial
C8 = 82pF
C9 = 330pF
C10 = 560pF
C11 = 2µF2/16V radial
C15 = 10µF/16V radial
C16 = 100µF/16V radial
C17 = 100nF SMT

Inductors:
L1 = 100µH

Semiconductors:
D1;D2 = LED
D3;D4 = 1N4148
D5 = 1N4001
T1 = BC557
T2;T3 = BC547
IC1 = 27C64 (order code 6331; see page 70)
IC2 = 7805
IC3 = SAA6579T (Philips Components)[1]
IC4 = 68HC05E0FN (Motorola)

Miscellaneous:
JP1 = 3-way SIL header with jumper.
K1;K3 = 10-way boxheader, angled.
K2 = 14-way boxheader, angled.
K4 = 2-way PCB terminal block, raster 7.5mm.
K5 = 2-way PCB terminal block, raster 5.0mm.
S1;S2 = on/off switch.
X1 = 4.000MHz crystal.
X2 = 4.332MHz crystal [1].
Re1 = PCB mount relay, coil voltage 12V, e.g., Siemens V23127-A2-A101.
Bz1 = 12V buzzer.
1 off 68-way PLCC socket.
4 off Digitast press-key [1].
1 off LCD module, 1x16 (LM015A) or 2x16 (LM016A) [1] or
1 off VFD module.
1 off Telet case type LC850 (60x200x132mm).
1 off printed circuit board and programmed EPROM; set order code 930121, see page 70).

[1] C-I Electronics, P.O. Box 22089, 6360 AB, Nuth, Holland. Fax +31 45 241877.

the display (LCD or VFD).

Start the construction by fitting the SAA6579T, which is an SMT (surface mount technology) component. This job requires a low-power soldering iron with a fine tip. Make sure of the orientation, because the IC is very difficult to remove once all pins are soldered. Some desoldering braid should be kept handy in case adjacent pins are accidentally connected by excess solder. Next, mount all passive components, such as resistors, capacitors, the relay and the connectors. Fit IC sockets in positions IC_1 and IC_4. Do not forget the SMT capacitor, C_{17}, which is fitted at the **solder** side of the board, underneath IC.

Before you proceed with the rest of the construction, have a good look at the HF section of the circuit. To make sure that the operation of the sensitive HF circuit is not upset by digital signals emanating from the microprocessor section, the RDS demodulator (IC_3 and associated components) is completely screened. The screen is made from 1.5 to 2 cm wide thin metal sheet, which is bent into shape and then soldered onto the PCB, after the HF parts have been fitted. The screen is soldered to six solder pins, at a height of about 0.5 mm above the board surface. The shape of the screen is indicated by the dashed lines on the component mounting plan.

Although it makes more sense to mount them behind the front panel of the RDS decoder case, LEDs D_1 and D_2 may also be soldered onto the printed circuit board for testing purposes. The four press-keys, ON/OFF, Alarm, RDS(+) and Sleep(-) are mounted on a small piece of veroboard or stripboard, which is secured to the inside of the enclosure front panel with the keys protruding at the front side. Alternatively, the switches may be glued into suitably drilled holes in the front panel. As shown by the circuit diagram, the wiring of the switches is extremely simple.

If an LCD display is used, this must be connected to K_2. When the LM015

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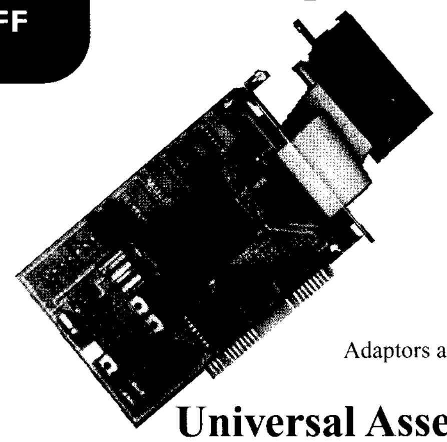

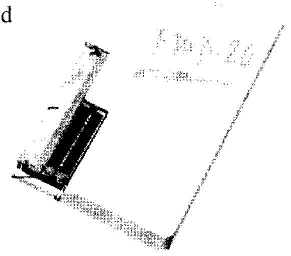

or LM016 is used, the link is simple because it is 'straight through' for all 14 connections (pin 1 to pin 1, etc.). Next, set jumper JP_1 as required (see above).

Figure 2 also shows how to connect a VF display. Note that this requires a separate supply to furnish the filament voltage and the high voltage.

A suggested front panel layout for the RDS decoder is given in **Fig. 5.** Having checked the construction and fitted the board into the case, all that remains to be done is adjust preset P_1 and trimmer C_3.

After applying power (use a 12V/150mA mains adaptor), the LCD display will show a text, which may be a bit difficult to read owing to poor contrast. Adjust preset P_1 for optimum contrast. This adjustment is not necessary if a VF display is used.

In most cases, trimmer capacitor C_3 can be set to the centre of its travel. Adjustment is only required if the clock is not accurate when no RDS signal has been received for a relatively long period. In this way, the clock deviation may eventually be eliminated.

Once the MPX signal is connected to the decoder input, the RDS information will appear on the display. That is, if your radio is tuned a station transmitting RDS, which is indicated by LED D_1 going out. ■

References:

1. EBU technical document 3244: Specifications of the Radio Data System, RDS, for VHF/FM Sound Broadcasting.

2. Radio Data System (RDS) demodulator. *Elektor Electronics* May 1989.

3. Radio Data System (RDS) decoder. *Elektor Electronics* February 1991.

4. RDS demodulator with integrated filter. *Elektor Electronics* October 1992.

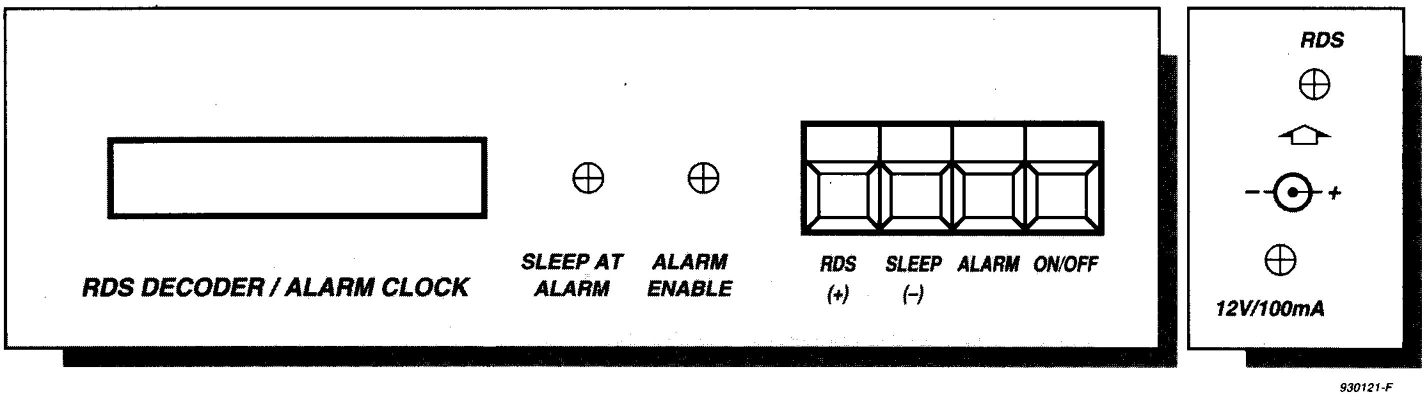

Fig. 5. Suggested front and rear panel layouts (shown at 78% of true size).

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COMMODORE 64 Customer returns but ok for spares etc £12 REF: MAG12P2 Tested and working units are £69.00 REF: MAG69

COMMODORE 64 TAPE DRIVES Customer returns at £4 REF: MAG4P9 Fully tested and working units are £12 REF: MAG12P5

COMPUTER TERMINALS complete with screen, keyboard and RS232 input/output. Ex equipment. Price is £27 REF: MAG27

MAINS CABLES These are 2 core standard black 2 metre mains cables fitted with a 13A plug on one end, cable the other. Ideal for projects, low cost manufacturing etc. Pack of 10 for £3 REF: MAG3P8 Pack of 100 £20 REF: MAG20P5

SURFACE MOUNT STRIPPER Originally made as some form of high frequency amplifier (main chip is a TSA5511T 1.3GHz synthasiser) but good stripper value, an excellent way to play with surface mount components £1.00 REF: MAG1P1.

MICROWAVE TIMER Electronic timer with relay output suitable to make enlarger timer etc £4 REF: MAG4P4

PLUG 420? showing your age? pack of 10 with leads for £2 REF: MAG2P11

MOBILE CAR PHONE £5.99 Well almost! complete in car phone excluding the box of electronics normally hidden under seat. Can be made to illuminate with 12v also has built in light sensor so display only illuminates when dark. Totally convincing! REF: MAG6P6

ALARM BEACONS Zenon strobe made to mount on an external bell box but could be used for caravans etc. 12v operation. Just connect up and it flashes regularly) £5 REF: MAG5P11

FIRE ALARM CONTROL PANEL High quality metal cased alarm panel 350x165x80mm. Comes with electronics but no information. £15 REF: MAG15P4

SUPER SIZE HEATSINK Superb quality aluminium heatsink. 365 x 183 x 61mm, 15 fins enamble high heat dissipation. No holes! £9.99 REF: MAG10P1P

REMOTE CONTROL PCB These are receiver boards for garage door opening systems. You may have another use? £4 ea REF: MAG4P5

LOPTX Line output transformers believed to be for hi res colour monitors but useful for getting high voltages from low ones! £2 each REF: MAG2P12 bumper pack of 10 for £12 REF: MAG12P3.

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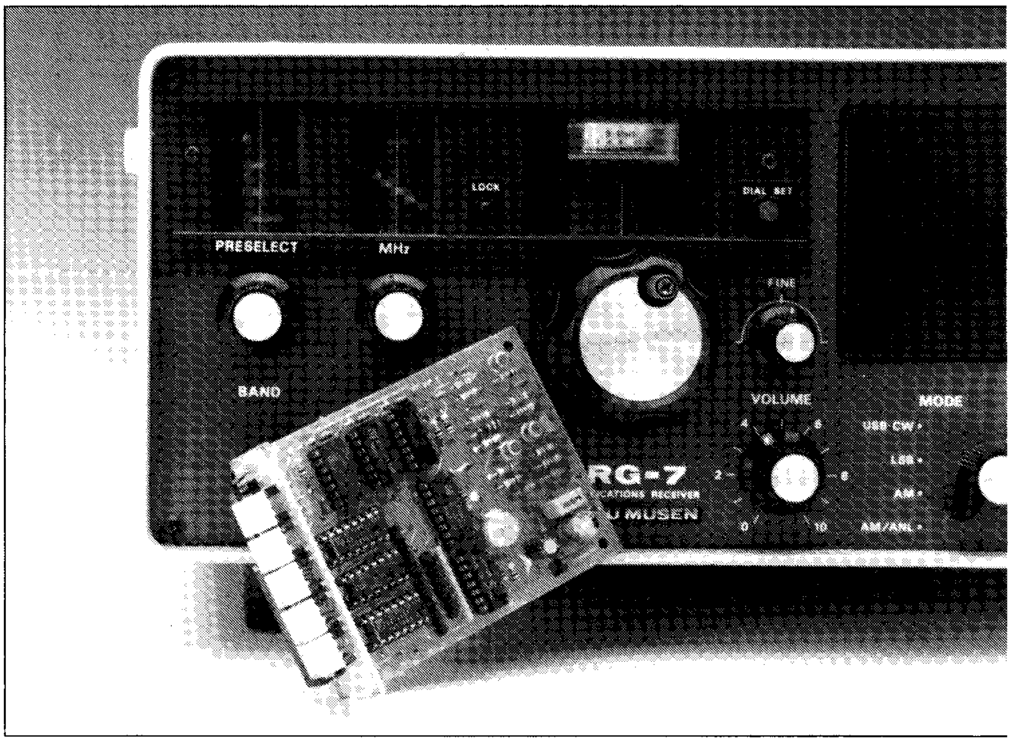
£49.99

A Hand held personal Gamma and X Ray detector. This unit contains two Geiger Tubes, has a 4 digit LCD display with a Piezo speaker, giving an audio visual indication. The unit detects high energy electromagnetic quanta with an energy from 30K eV to over 1.2M eV and a measuring range of 5-9999 UR/h or 10-99990 Nr/h. Supplied complete with handbook.

REF: MAG50

DIGITAL DIAL

There is a vast number of communication receivers around that have an analogue (needle and dial) tuning scale. Although the RF performance of many ex-army and other surplus receivers (whether valve, transistor, or 'hybrid') is quite acceptable for radio amateur use, their tuning scales and mechanically operated dials are really old fashioned these days, and in for 'digital' revision.



From a basic design by David McBright

ALTHOUGH their number seems to have decreased considerably since the nineteen seventies, ex-army communication receivers from the Second World War and the Cold War years are still to be found in electronic surplus stores, and at radio amateur rallies. An example of a very popular surplus receiver is the BC348, which was once used in the B17 'flying fortress' bomber. Only a few modifications are required to make this receiver suitable for radio amateur use, in particular, for reception of SSB (single-sideband) and narrow-band FM (frequency modulation). Since the short-wave bands covered by receivers like the BC348 are pretty crowded these days, there is a clear need of an improved (digital) frequency readout. This allows you to tune the receiver as accurately as possible, 'dredging' the station you want to hear from the noise and interference caused by other, stronger, stations.

A serious problem with older receivers is the wide variety of first and second intermediate frequencies (IFs) used. This means that the digital dial we are about to describe must be designed such that it can be used with many different local oscillator (LO) frequencies and output levels.

The circuit proposed here has everything to meet the above requirements, and more: low power consumption, a crystal-controlled timebase, and an IF offset which can be programmed to any value between 0 and 1.6 MHz in steps of 1 kHz. The offset frequency may be subtracted from the LO frequency, or added to the LO frequency, depending on whether the LO frequency is above ('LO-high') or below ('LO-low') the frequency of the received signal.

The digital dial has a frequency range of up to 39.999 MHz at a resolution of 1 KHz. The display refresh rate is 4 Hz.

The circuit

The circuit diagram of the digital dial is given in **Fig. 1**. The circuit is based on inexpensive and commonly available components only. To make sure that the tuning frequency can be read under all circumstances, a bright orange 4½-digit LED display is used. Circuit IC_{10}, an ICM7217AIPI from Intersil (Harris Semiconductors), controls four display segments. The most significant display segment is driven by IC_7, a 4543. In this configuration, the highest counter state is 39,999, which is composed as follows: 0 (blanked), 1, 2 or 3 via LD_1 and IC_7, and 0000 to 9999 via the displays driven by IC_{10}. The five digits form a separate unit, together with IC_7, IC_{10} and connector K_3, to allow the display to be mounted in the best visible position when it is fitted into the receiver.

The performance of the circuit is determined to a large extent by the sensitivity and the frequency range of the input amplifier. Here, the input amplifier consists of three low-cost transistors type BSX20. These fast switching transistors can be used without problems in the frequency range of the present circuit because their cut-off frequency is specified at 500 MHz. An alternative to the BSX20 is the Zetex E-line ZTX313. The input amplifier has a relatively high input impedance, so that it has virtually no effect if a characteristic impedance of 75 Ω is used to couple the LO signal to the digital dial. The highest input level that may be applied without the transistors going into saturation is about 4 V_{pp}. In principle, it is possible to increase the sensitivity of the input amplifier, so that signals with a level smaller than 100 mV_{pp} or even lower can be measured. Unfortunately, increasing the sensitivity will result in a narrower input bandwidth.

According to the datasheets, the HCMOS digital circuits used here operate at the highest possible speed at a supply voltage of about 6 V. For HCT ICs, this specification is about 5.5 V. Hence, the supply voltage in the present circuit is raised a little above the usual 5 V, to 5.6 V. Arguably, this is a reasonable compromise between a long IC life expectancy and high speed. As a matter of interest, both HC and HCT ICs are beginning to have a hard time at supply voltages above 7 V.

The timebase

The central part in the timebase is an inexpensive, yet highly accurate,

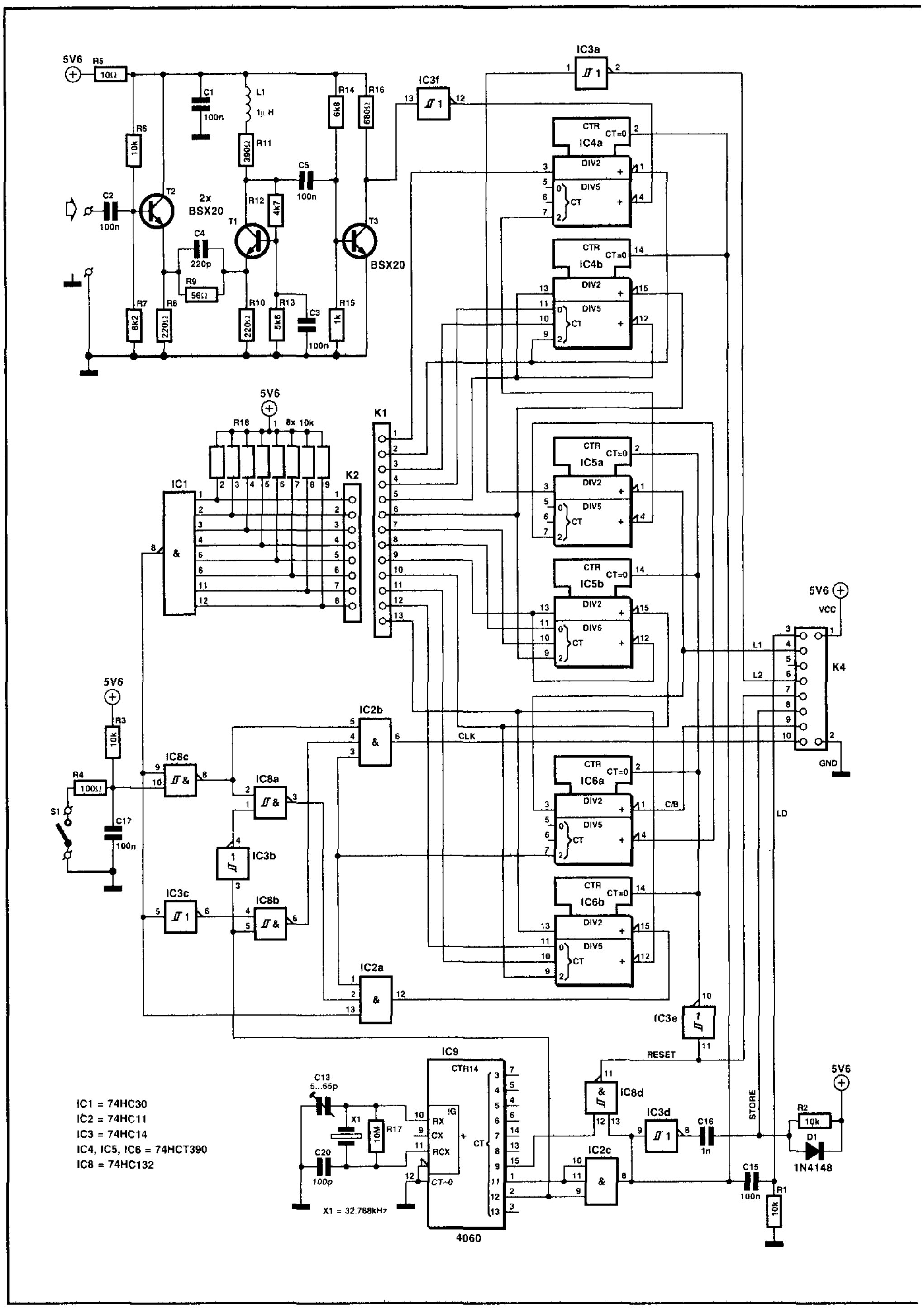


Fig. 1. Circuit diagram of the multi-purpose digital dial for communication receivers.

32.768 kHz digital watch crystal, X_1. The oscillator signal generated with the aid of this crystal is scaled down by a 4060 to give the required clock signals. Dividing 32.768 kHz by 2^{13} yields a signal with a frequency of 4 Hz. The half period time of this signal is 125 ms, which can be found on pin 2 (Q12), and is used to enable the counter. The second half of the period time, when the signal is low, ensures that the result of the counter operation is stored in the display.

It is readily seen that dividing the input signal by 125, and using a time-base gate of 125 ms, yields the input frequency in kilohertz (kHz). In this timing arrangement, the counter state is updated four times a second, which is ample for the present application.

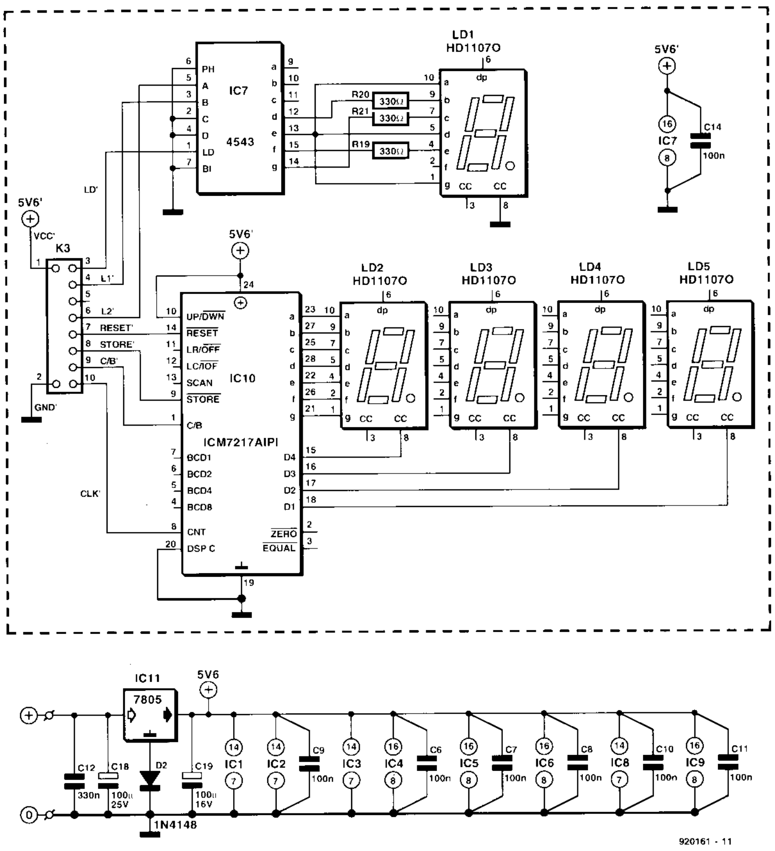
Apart from the 4 Hz gate signal, IC_9 also supplies 8-Hz and 16-Hz signals. The 4-Hz and 8-Hz signals are combined in gate IC_2, which consequently supplies a short pulse (62.5 ms) with a repeat rate of 4 Hz. A differentiating network, C_{15}-R_1, turns this signal into a needle-shaped pulse (LD) which is used to latch the information into IC_7. The short 4-Hz signal is also used to generate a store pulse for IC_{10}. This is achieved with the aid of a buffer, IC_3, and a second differentiating network, R_2-C_{16}. Gate IC_{8d} combines the 16-Hz signal with the output signal of IC_{2c} to give an even shorter pulse (31.25 ms) with a frequency of 4 Hz. This signal is used to reset IC_5, IC_6 and IC_7 four times a second. IC_4 is reset directly by IC_{2c}.

The display circuit is contained in the dashed box in the circuit diagram. IC_7 drives the first of the four display digits, which shows 1, 2, 3 or nothing. The zero that would normally appear when IC_7 receives a 0 is ingeniously suppressed by a purposely incorrect segment connection order. The number that appears on the display is determined by drive lines L1 and L2. The logic levels on these lines are, in turn, determined by the number of carry/borrow (C/B) pulses generated by integrated counter IC_{10}. These pulses also arrive at IC_5 via counter IC6. Both binary scalers supply their output signal to IC_7. Next, the arrival of the LD pulse causes the bit combination to be stored into IC_7, and the desired segments of LD_1, a HD11070, to light.

Most of the counting work is done by IC_{10}, a complex integrated counter Type ICM7217 from Intersil (Harris Semiconductor). This IC is capable of counting from 0000 to 9999. The C/B output of the ICM7217 signals an overflow in the counter. The store pulse applied to pin 9 determines when the counter state is transferred to the display. The multiplexing of the four segments is also done by the electronics contained in the ICM7217. A reset pulse at pin 14 clears the input of the counters, and resets the display to zero. Unfortunately, IC_7 can not be reset to zero with the aid of a reset pulse, so that a different way of doing this has to be devised. The contents of IC_7 are cleared by supplying the IC with an LD pulse, after the counters to which it is connected are reset. Consequently, a value of nought is stored in the driver, and the LED display goes dark again.

Three dual decade counters Type 74HCT390 are used to divide the RF signal, and implement the offset compensation. The counters may be divided into two sections which divide by 2 and 5 respectively. Further, they share a reset input.

As already mentioned, a total scale factor of 125 is required. This is fairly simple to achieve by cascading three divide-by-five scalers. The LO-high and LO-low correction is realized by varying the gate time. When LO-high use is required, the gate time is lengthened with an extra measurement period which is deduced from the desired offset. Similarly, the gate time is shortened when LO-low use is in order. Switch S_1 is used to select between LO-low and LO-high. The gate time can vary by ±62.5 kHz. On the display, this means that a margin of 0000 kHz to



1,999 kHz is available to compensate the frequency offset of the local oscillator.

The counting operation

Since four measurements are taken every second, a period of 250 ms is available for each complete measurement cycle. The first half period (125 ms) is reserved for counting, while the second half period is available for updating the display. As already mentioned, the input signal needs to be divided by 125 to obtain the correct measured value in kHz within the gate time of 125 ms.

Further, the counter has to take care of the IF offset. This is achieved by adding or subtracting a certain number of pulses to or from the measured value. The counter circuit consists of IC$_4$, IC$_5$ and IC$_6$. These ICs are connected in a fairly complex way because they have two functions. Consequently, the operation of the counter may not be obvious straight away.

The Type 74HC390 IC (of which there are three in the counter circuit) consists of two identical blocks which will be designated IC$_{xA}$ and IC$_{xB}$ for the sake of convenience. One block uses the high pin numbers, the other, the low pin numbers. Each block consists of a divide-by-two and a divide-by-five counter, which form a (BCD) decade counter when cascaded. The two counters are linked by connecting output Qa (pin 3 or 13) of the divide-by-two section to the clock input (pin 4 or 12) of the divide-by-five counter.

The input signal reaches the input of the divide-by-five counter in IC$_{4a}$ via inverter IC$_{3f}$. This counter is connected in series with, successively, the divide-by-five counters in IC$_{5a}$ and IC$_{6a}$. This gives a total scale factor of 125. Depending on the two control signals at the other inputs of IC$_{2b}$, the output signal is fed to the integrated counter/display driver, IC$_{10}$. This signal is also fed to the offset counter via IC$_{2a}$. The offset counter consists of three series connected BCD counters, IC$_{4b}$, IC$_{5b}$ and IC$_{6b}$. To realize an extra digit, these counters are followed by the divide-by-two section in IC$_{4a}$. In this setup, the 13 outputs of the offset counter allow any desired IF frequency (offset) to be set in steps of 1 kHz.

The output of NAND gate IC$_1$ goes low as soon as the desired offset is reached. This means that pin 13 of IC$_{2a}$ is first high, and that the passing or blocking of the clock pulses depends on the level at pin 2 of this gate only. The offset counter is disabled as soon as the programmed offset value is reached.

LO-low use (LO frequency below that of the received signal) is selected by closing switch S$_1$. The output of IC$_{8c}$ is then always high, while IC$_{8b}$ controls the flow or interruption of clock pulses to IC$_{10}$. The output of IC$_{8b}$ is high as long as the offset counter has not reached its end value. However, the offset counter is disabled via IC$_{8a}$, and not enabled again until pin 2 of IC$_9$ goes logic high. Consequently, IC$_{10}$ continues to receive pulses after the measurement cycle. The result is that the offset is added to the measurement value.

When switch S$_1$ is opened, the digital dial is programmed for LO frequencies above those of the received RF signals. The opened switch causes the pulses for IC$_{10}$ to be blocked by IC$_{8c}$ at the start of a measurement cycle. During this time, the offset counter is enabled. This counter stops as soon as the programmed offset value is reached, whereupon clock pulses are fed to IC$_{10}$. Effectively, the offset value is subtracted from the measured value.

The binary counters in IC$_{5a}$ and IC$_{6a}$ are used to drive display LD$_1$. This fairly unusual approach allows the leading zero to be suppressed. The leading zero suppression on IC$_{10}$ is switched off since there is no connection with the highest digit of the display.

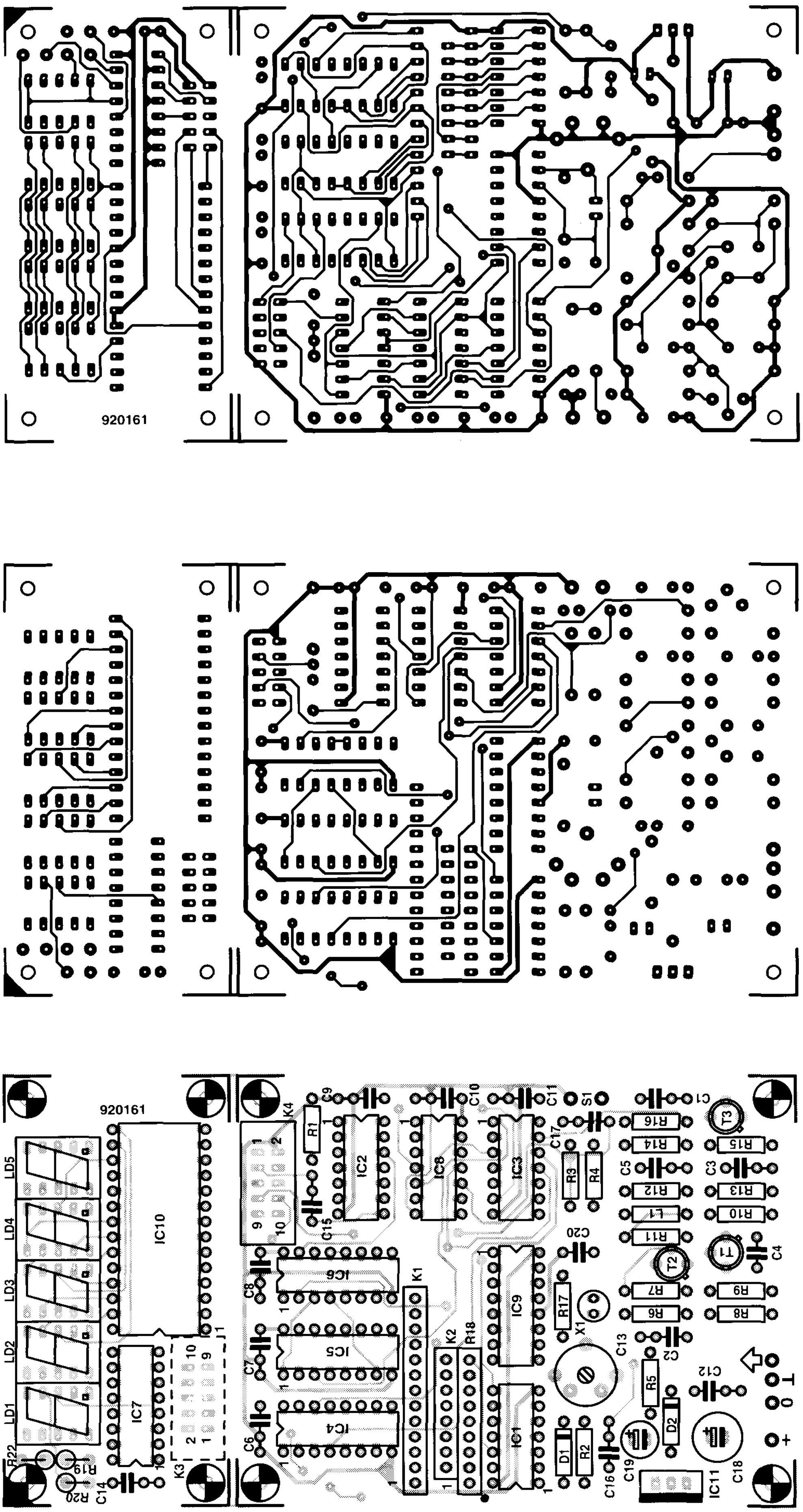


Fig. 2. Copper track layouts (direct reading) and component mounting plan of the double-sided PCB designed for the digital dial.

COMPONENTS LIST

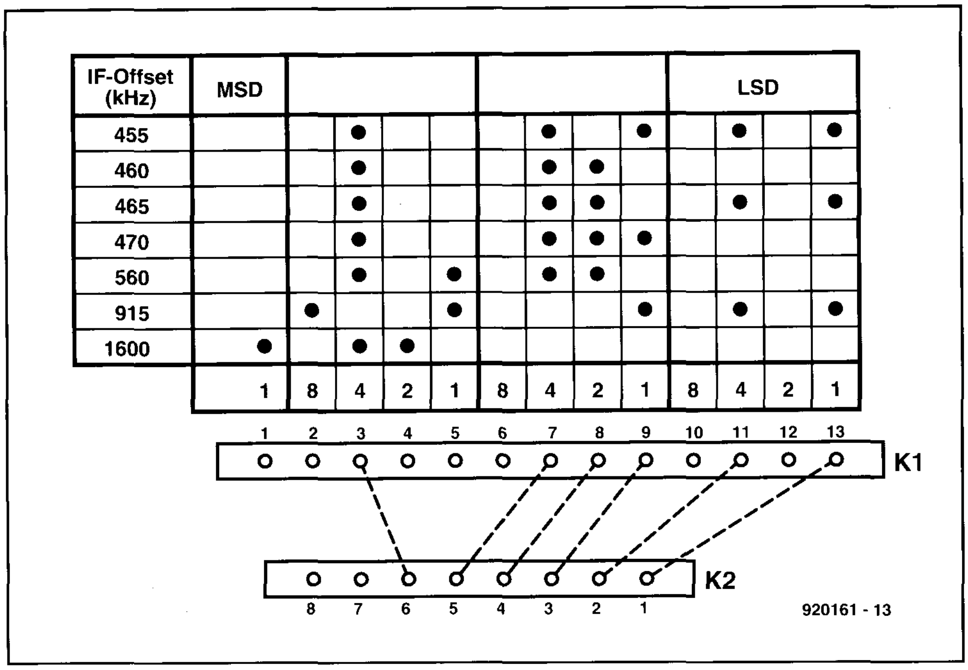
Resistors:
R1;R2;R3;R6 = 10kΩ
R4 = 100Ω
R5 = 10Ω
R7 = 8kΩ2
R8;R10 = 220Ω
R9 = 56Ω
R11 = 390Ω
R12 = 4kΩ7
R13 = 5kΩ6
R14 = 6kΩ8
R15 = 1kΩ
R16 = 680Ω
R17 = 10MΩ
R18 = 8-way SIL array 10kΩ
R19;R20;R21 = 330Ω

Capacitors:
C1;C2;C3;C5-C11;C14;C15;C17 = 100nF
C4 = 220pF
C12 = 330nF
C13 = 65pF trimmer
C16 = 1nF
C18 = 100µF/25V radial
C19 = 100µF/16V radial
C20 = 100pF

Inductor:
L1 = 1µH

Semiconductors:
D1;D2 = 1N4148
T1;T2;T3 = BSX20
IC1 = 74HC30
IC2 = 74HC11
IC3 = 74HC14
IC4;IC5;IC6 = 74HCT390
IC7 = 4543
IC8 = 74HC132
IC9 = 4060
IC10 = ICM7217AIPI
IC11 = 7805
LD1-LD5 = HD11070

Miscellaneous:
K1 = 13-way pinheader.
K2 = 8-way pinheader.
K3/K4 = 10-way pinheader.
S1 = on/off switch.
X1 = 32.768kHz crystal.
Printed circuit board 920161 (see page 70).



IF-Offset (kHz)	MSD									LSD			
455			●				●		●		●		●
460			●				●	●					
465			●				●	●			●		●
470			●				●	●	●				
560			●		●		●	●					
915		●			●				●		●		●
1600	●		●	●									
	1	8	4	2	1	8	4	2	1	8	4	2	1

Fig. 3. Examples showing how to program the IF offset compensation.

Construction

The digital dial is best built on the printed circuit board shown in **Fig. 2**. In view of the complexity of the track layout, and the high track density, we do not recommend etching this board yourself.

Separate the main board from the display section before you start fitting components. The display is a separate unit to enable it to be fitted at the most convenient position in the receiver, or at right angles on to the main board.

The use of IC sockets is recommended only to those of you who feel not so certain about their soldering skills. Although the circuit operates at fairly high frequencies, the construction is not critical. The passive parts are fitted first, then the active parts.

The resistors next to LD$_1$ are fitted upright to keep the display section as compact as possible. Make sure that the resistors do not protrude above the displays. If they do, the completed display board can not be fitted properly behind the front panel of the receiver. If the resistors are too large, either fit them at the track side of the board, or fit IC sockets for the displays.

Connector K$_3$ is fitted at the track side of the display board. K$_1$ and K$_2$ are two single-row pin headers. Alternatively, use small PCB solder terminals.

Once all components are accommodated on the boards, and the boards have been interconnected, the oscillator around X$_1$ may be adjusted, and the receiver IF offset programmed. The examples in **Fig. 3** provide information on programming the offset compensation. Obviously, you have to know the receiver's IF offset to be able to do the programming. In most cases, this is easy to find out from the documentation, or by looking for the print on the IF filter contained in the receiver. If you are still unable to ascertain the IF, simply tune to a station with a known frequency, and measure the local oscillator frequency. This will also tell you if the LO frequency is above or below the input signal frequency.

All that remains to be done at this point is fit the wire links between K$_1$ and K$_2$. The setting for a number of commonly used IFs is already given. The wiring example is based on the assumption that the IF frequency is 475 kHz. If you are faced with an unusual IF, you have to 'assemble' the four digits yourself. Look at the 475 kHz example; the last digit (LSD) is composed of 4+1, the second digit of 4+2+1, and the third of 4 only. A fourth digit is not necessary because it is 0. Hence, the 1 is not used. Having fitted the appropriate wires, you need to set S$_1$ for LO-low or LO-high. This selection should also be based on technical information you have available on the communications receiver, or on a measurement as mentioned above. Obviously, if the digital dial is always used in the same receiver, switch S$_1$ may be omitted or replaced by a wire link.

The finishing touch is, of course, fitting the digital dial into the communications receiver. Alternatively, some of you may wish to build the dial as a self-contained unit, i.e., in a separate enclosure. If this is done, the circuit is best powered by a mains adaptor with an output voltage of 8-15 V, and a current rating of 250 mA. The input of the circuit is connected to the local oscillator via a short length of coax cable. Some experimenting may be required to locate a 'tapping' point that does not cause oscillator detuning. If possible, go for light inductive coupling, since that is electrically safer than capacitive coupling (however light) in valve receivers.

Switch on the receiver, and tune to a known station. If necessary, correct the frequency readout on the digital dial by carefully adjusting trimmer C$_1$. From then on, the digital dial is ready for use. ■

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40193	**£0.60**

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All 2oz Reels

14 SWG	**£0.63**
16 SWG	**£0.67**
18 SWG	**£0.67**
20 SWG	**£0.72**
22 SWG	**£0.76**
24 SWG	**£0.80**
26 SWG	**£0.89**
28 SWG	**£0.91**
30 SWG	**£0.93**
32 SWG	**£0.93**
34 SWG	**£0.99**
36 SWG	**£1.04**
38 SWG	**£1.10**
40 SWG	**£1.22**

TRANSISTORS

2N1613	**£0.31**	BC186	**£0.33**	BD534	**£0.47**
2N1711	**£0.26**	BC204C	**£0.72**	BD535	**£0.48**
2N1893	**£0.29**	BC206B	**£0.72**	BD536	**£0.65**
2N2218A	**£0.28**	BC207C	**£0.72**	BD646	**£0.52**
2N2219A	**£0.25**	BC208	**£0.72**	BD648	**£0.52**
2N2222A	**£0.16**	BC209A	**£0.72**	BD650	**£0.53**
2N2646	**£0.80**	BC212	**£0.08**	BD707	**£0.42**
2N2904A	**£0.25**	BC212L	**£0.08**	BD807	**£0.80**
2N2905A	**£0.23**	BC212LB	**£0.08**	BDX32	**£1.78**
2N2907	**£0.20**	BC213	**£0.08**	BDX33C	**£0.46**
2N2926	**£0.16**	BC213LC	**£0.08**	BDX34C	**£0.50**
2N3053	**£0.27**	BC214	**£0.08**	BDX53C	**£0.47**
2N3054	**£0.90**	BC214L	**£0.08**	BDX54C	**£0.50**
2N3055	**£0.62**	BC237B	**£0.09**	BF180	**£0.31**
2N3440	**£0.50**	BC238C	**£0.09**	BF182	**£0.31**
2N3702	**£0.09**	BC239C	**£0.10**	BF185	**£0.31**
2N3703	**£0.10**	BC251	**£0.13**	BF194	**£0.19**
2N3704	**£0.10**	BC252	**£0.13**	BF195	**£0.19**
2N3705	**£0.10**	BC261B	**£0.24**	BF244	**£0.35**
2N3706	**£0.10**	BC262B	**£0.24**	BF257	**£0.33**
2N3771	**£1.44**	BC267B	**£0.30**	BF259	**£0.33**
2N3772	**£1.51**	BC307	**£0.10**	BF337	**£0.36**
2N3773	**£1.79**	BC308	**£0.10**	BF355	**£0.38**
2N3819	**£0.40**	BC327	**£0.10**	BF423	**£0.13**
2N3820	**£0.58**	BC328	**£0.10**	BF451	**£0.19**
2N3904	**£0.10**	BC337	**£0.10**	BF459	**£0.29**
2N3905	**£0.10**	BC338	**£0.10**	BF469	**£0.36**
2N3906	**£0.10**	BC414C	**£0.13**	BFX29	**£0.29**
2N4036	**£0.31**	BC441	**£0.40**	BFX84	**£0.31**
2N5296	**£0.57**	BC461	**£0.40**	BFX85	**£0.31**
2N5321	**£0.57**	BC463	**£0.29**	BFY50	**£0.29**
2N6107	**£0.60**	BC478	**£0.32**	BFY51	**£0.26**
AC126	**£0.30**	BC479	**£0.32**	BFY52	**£0.28**
AC127	**£0.30**	BC490	**£0.24**	BS107	**£0.21**
AC128	**£0.28**	BC516	**£0.22**	BS170	**£0.21**
AC187	**£0.45**	BC517	**£0.20**	BSW66	**£1.35**
AC188	**£0.37**	BC527	**£0.20**	BU126	**£1.70**
ACY17	**£3.84**	BC528	**£0.20**	BU205	**£1.82**
AD149	**£1.67**	BC537	**£0.20**	BU208A	**£1.73**
AD161	**£0.92**	BC546C	**£0.08**	BU326A	**£1.80**
AD162	**£0.92**	BC547C	**£0.09**	BU500	**£2.32**
BC107	**£0.14**	BC548C	**£0.08**	BU508A	**£1.76**
BC107B	**£0.15**	BC549C	**£0.10**	BU526	**£2.24**
BC108	**£0.13**	BC550C	**£0.08**	BU806	**£1.36**
BC108A	**£0.14**	BC556A	**£0.08**	BUX84	**£0.77**
BC108C	**£0.14**	BC557C	**£0.08**	IRF540	**£1.60**
BC109	**£0.14**	BC558C	**£0.08**	IRF740	**£1.63**
BC109C	**£0.15**	BC559C	**£0.08**	MJ11015	**£2.11**
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BC115	**£0.41**	BC637	**£0.21**	MJ2501	**£1.60**
BC116	**£0.41**	BC638	**£0.21**	MJ3001	**£1.52**
BC118	**£0.41**	BC639	**£0.21**	MJE340	**£0.40**
BC132	**£0.36**	BC640	**£0.21**	MJE350	**£0.42**
BC134	**£0.36**	BCY70	**£0.21**	MPSA13	**£0.12**
BC135	**£0.36**	BCY71	**£0.20**	MPSA42	**£0.17**
BC140	**£0.25**	BCY72	**£0.20**	MRF475	**£6.21**
BC141	**£0.27**	BD135	**£0.20**	TIP121	**£0.35**
BC142	**£0.31**	BD136	**£0.21**	TIP122	**£0.37**
BC143	**£0.34**	BD137	**£0.22**	TIP125	**£0.37**
BC149	**£0.12**	BD138	**£0.22**	TIP127	**£0.37**
BC154	**£0.36**	BD139	**£0.23**	TIP132	**£0.46**
BC157	**£0.12**	BD140	**£0.24**	TIP137	**£0.46**
BC159	**£0.12**	BD150C	**£0,82**	TIP142	**£1.06**
BC160	**£0.28**	BD165	**£0.42**	TIP147	**£1.12**
BC170	**£0.16**	BD166	**£0.35**	TIP2955	**£0.63**
BC170B	**£0.16**	BD187	**£0.39**	TIP29C	**£0.31**
BC171	**£0.11**	BD201	**£0.40**	TIP3055	**£0.63**
BC171B	**£0.16**	BD202	**£0.40**	TIP30C	**£0.31**
BC172	**£0.13**	BD203	**£0.40**	TIP31C	**£0.32**
BC172B	**£0.13**	BD204	**£0.40**	TIP32C	**£0.32**
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BC182	**£0.08**	BD237	**£0.32**	TIP47	**£0.48**
BC182L	**£0.08**	BD238	**£0.32**	TIP48	**£0.62**
BC182LB	**£0.08**	BD240B	**£0.37**	TIP50	**£0.53**
BC183	**£0.08**	BD243B	**£0.50**	VN10KM	**£0.44**
BC183L	**£0.08**	BD244A	**£0.53**	VN66AF	**£1.50**
BC183LB	**£0.08**	BD246	**£1.06**	ZTX300	**£0.16**
BC184	**£0.08**	BD441	**£0.41**	ZTX500	**£0.16**
BC184L	**£0.08**	BD442	**£0.41**		

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78L12	**£0.24**
78L15	**£0.24**
79L05	**£0.28**
79L12	**£0.28**
79L15	**£0.28**
7805	**£0.28**
7812	**£0.28**
7815	**£0.28**
7905	**£0.38**
7912	**£0.38**
7915	**£0.38**
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5mm Red LED	**£0.09**
5mm Green LED	**£0.10**
5mm Yellow LED	**£0.10**
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3mm Green LED	**£0.12**
3mm Yellow LED	**£0.13**
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common anode	**£1.14**
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TIC106D	**£0.40**
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ELECTROLYTIC RADIAL CAPACITORS

uF	16V	25V	63V	100V	450V
0.47	–	–	**£0.05**	**£0.07**	–
1.0	–	–	**£0.05**	**£0.06**	**£0.15**
2.2	–	–	**£0.05**	**£0.06**	**£0.18**
4.7	–	–	**£0.05**	**£0.08**	**£0.30**
10	**£0.05**	**£0.05**	**£0.06**	**£0.08**	**£0.48**
22	**£0.05**	**£0.05**	**£0.09**	–	–
47	**£0.06**	**£0.06**	**£0.11**	–	–
100	**£0.06**	**£0.09**	**£0.11**	–	–
220	**£0.09**	**£0.12**	**£0.31**	–	–
470	**£0.15**	**£0.19**	**£0.57**	–	–
1000	**£0.22**	**£0.29**	–	–	–
2200	**£0.37**	**£0.57**	–	–	–
4700	–	**£1.11**	–	–	–

ELECTROLYTIC AXIAL CAPACITORS

uF	16V	25V	63V	100V	450V
0.47	–	–	–	**£0.15**	–
1.0	–	–	**£0.10**	**£0.10**	**£0.19**
2.2	–	–	**£0.10**	**£0.10**	**£0.22**
4.7	–	**£0.09**	**£0.10**	**£0.10**	**£0.34**
10	–	**£0.12**	**£0.12**	**£0.12**	**£0.48**
22	–	**£0.09**	**£0.13**	**£0.17**	**£1.06**
47	**£0.10**	**£0.11**	**£0.16**	**£0.20**	**£1.33**
100	**£0.10**	**£0.13**	**£0.21**	–	**£2.46**
220	**£0.13**	**£0.18**	**£0.42**	–	–
470	**£0.21**	**£0.24**	**£0.69**	–	–
1000	**£0.33**	**£0.40**	**£1.05**	–	–
2200	**£0.52**	**£0.64**	–	–	–
4700	**£0.90**	–	–	–	–

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CA555	**£0.22**
CA741CE	**£0.18**
CA747CE	**£0.39**
CA3046	**£0.37**
CA3080	**£0.72**
CA3130	**£0.98**
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CA3140	**£0.56**
CA3240	**£1.22**
ICL7621	**£1.70**
ICM7555	**£0.43**
ICM7556	**£0.96**
LM301A	**£0.25**
LM348N	**£0.31**
LF351N	**£0.36**
LF353	**£0.41**
LM358N	**£0.27**
LM377	**£2.57**
LM380N	**£1.12**
LM381	**£2.70**
LM386	**£0.48**
LM387	**£1.60**
LM392N	**£0.79**
LM393N	**£0.28**
LM748CN	**£0.31**
LM1458	**£0.26**
LM3900	**£0.72**
LM3914	**£2.70**
LM3915	**£2.70**
MC3340	**£1.60**
MC4558	**£0.36**
NE531	**£1.56**
NE556N	**£0.36**
NE567N	**£0.36**
NE5532	**£0.80**
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TBA820M	**£0.39**
TDA2030	**£1.35**
TL061	**£0.35**
TL062	**£0.42**
TL064	**£0.46**
TL071CP	**£0.32**
TL072CP	**£0.34**
TL074CN	**£0.48**
TL081	**£0.33**
TL082CP	**£0.34**
TL084CN	**£0.46**
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ZN426E	**£2.61**
ZN427E	**£8.82**
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2716	**£4.46**
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6264-10	**£3.06**
62256-10	**£4.83**
4164-15	**£1.78**
41256-10	**£2.80**
511000-8	**£5.61**
514256-8	**£5.61**

DIL SOCKETS

8 Pin	**£0.07**
14 Pin	**£0.11**
16 Pin	**£0.15**
18 Pin	**£0.15**
20 Pin	**£0.16**
24 Pin	**£0.19**
28 Pin	**£0.22**
40 Pin	**£0.25**

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M 12 Watt	**£7.75**
C 15Watt	**£7.78**
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Desolder Pump	**£3.00**
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22SWG 0.5Kg Solder	**£7.40**
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1mm 3 yds Solder	**£0.62**
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BNC Solder Plug 50R	**£0.93**
BNC Solder Plug 75R	**£0.96**
BNC Crimp Plug 50R	**£0.68**
BNC Crimp Plug 75R	**£0.68**
BNC Solder Skt	**£1.08**
BNC Chassis Skt	**£0.80**
PL259 5.2mm	**£0.68**
PL259 11mm	**£0.62**
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64mm x 95mm	**£0.90**
64mm x 431mm	**£3.22**
95mm x 127mm	**£1.50**
95mm x 95mm	**£1.10**
95mm x 431mm	**£4.80**
100mm x 160mm	**£1.60**
119mm x 454mm	**£6.20**

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81mm x 60mm	**£3.06**
175mm x 42mm	**£3.74**
175mm x 67mm	**£5.56**
203mm x 75mm includes mounting plate & posts	**£7.36**

COPPER BOARD (G. Fibre)

100mm x 160mm	**£0.90**
110mm x 220mm	**£1.24**

PHOTO RESIST BOARD (G. Fibre)

3" x 4"	**£0.86**
4" x 6"	**£1.62**
4" x 8"	**£2.09**
6" x 6"	**£2.41**

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3" x 4"	**£0.67**
4" x 6"	**£1.24**
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1.0pF to 100nF
1pF-1nF **£0.06**, 1n2-2n7 **£0.07**,
3n3-4n7 **£ 0.12**,
10n & 12n **£0.07**
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47p-2n2 **£0.09**, 2n7-10n **£0.12**

D CONNECTORS

	Plug	Socket
9 Pin	**£0.29**	**£0.30**
15 Pin	**£0.39**	**£0.39**
15 Pin H.D.	**£0.81**	**£0.90**
23 Pin	**£0.40**	**£0.49**
25 Pin	**£0.48**	**£0.50**
9 Way plastic cover		**£0.30**
15 Way plastic cover		**£0.33**
23 Way plastic cover		**£0.36**
25 Way plastic cover		**£0.36**

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W005 1.5A 50V	**£0.19**
WO2 1.5A 200V	**£0.20**
BR32 3A 200V	**£0.36**
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SPST Toggle	**£0.58**
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9 Way D Female to Female	**£2.33**
9 Way D Male to Male	**£2.33**
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25 Way D Male to Male	**£2.71**
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1N4001	**£0.06**
1N4002	**£0.07**
1N4003	**£0.07**
1N4004	**£0.07**
1N4005	**£0.07**
1N4006	**£0.08**
1N4007	**£0.08**
1N5400	**£0.09**
1N5401	**£0.09**
1N5402	**£0.09**
1N5404	**£0.11**
1N5406	**£0.11**
1N5407	**£0.14**
1N5408	**£0.15**
1N914	**£0.06**
1N916	**£0.06**
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BY133	**£0.13**
OA47	**£0.28**
OA90	**£0.07**
OA91	**£0.10**
OA202	**£0.27**
BA157	**£0.10**
BA158	**£0.10**
BA159	**£0.10**
1N4149	**£0.06**
OA200	**£0.10**

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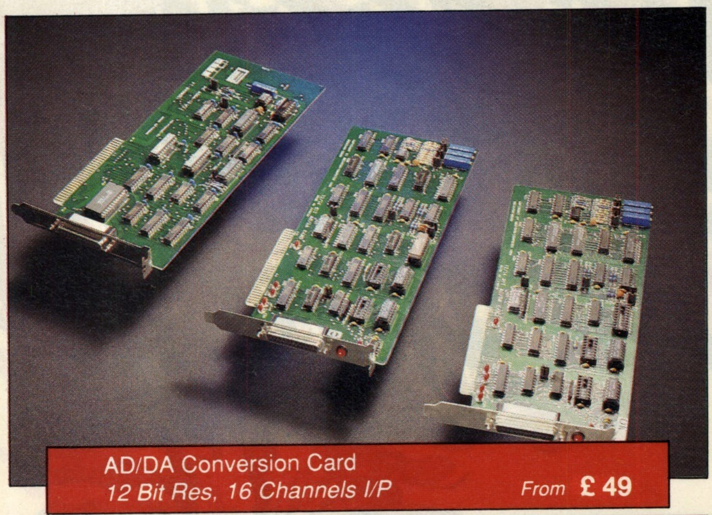

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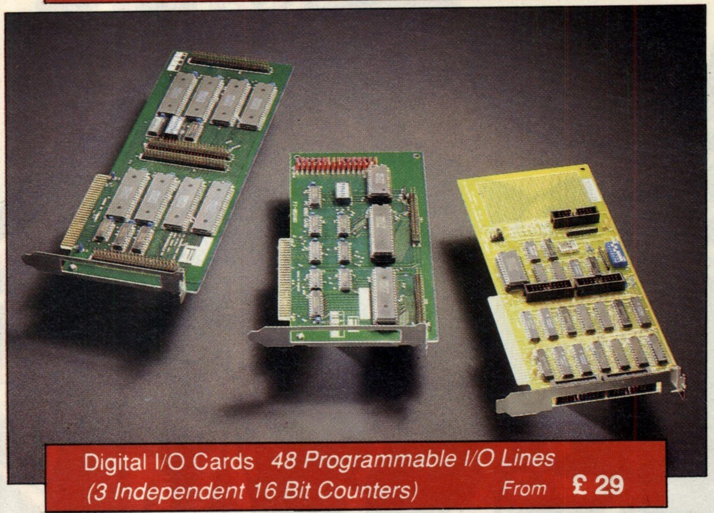

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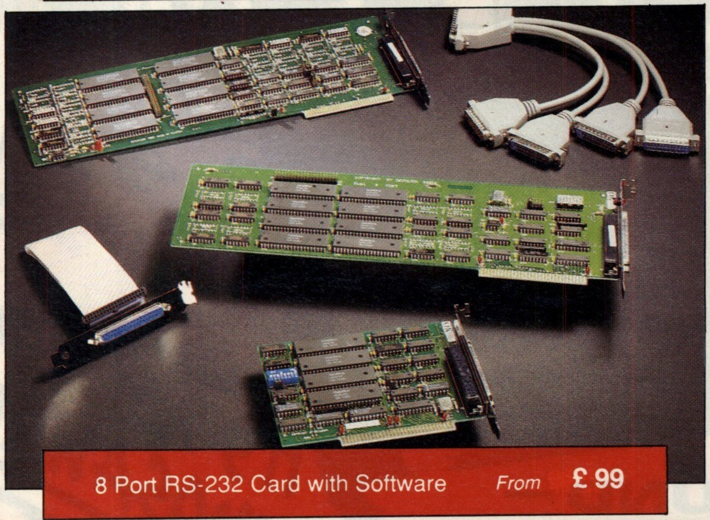

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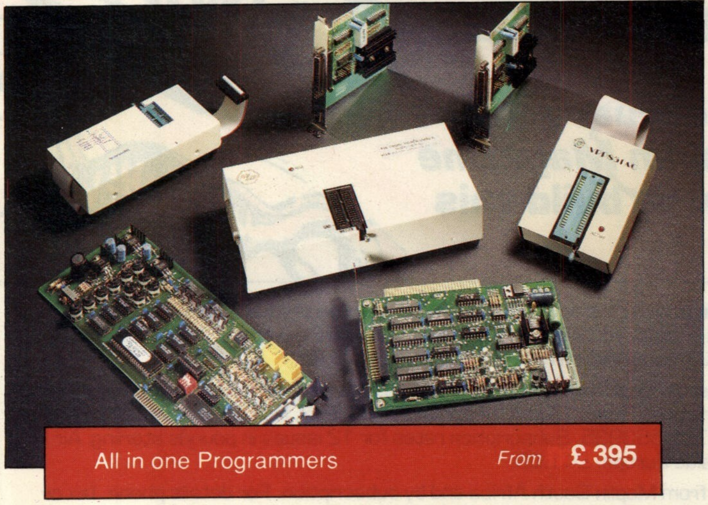

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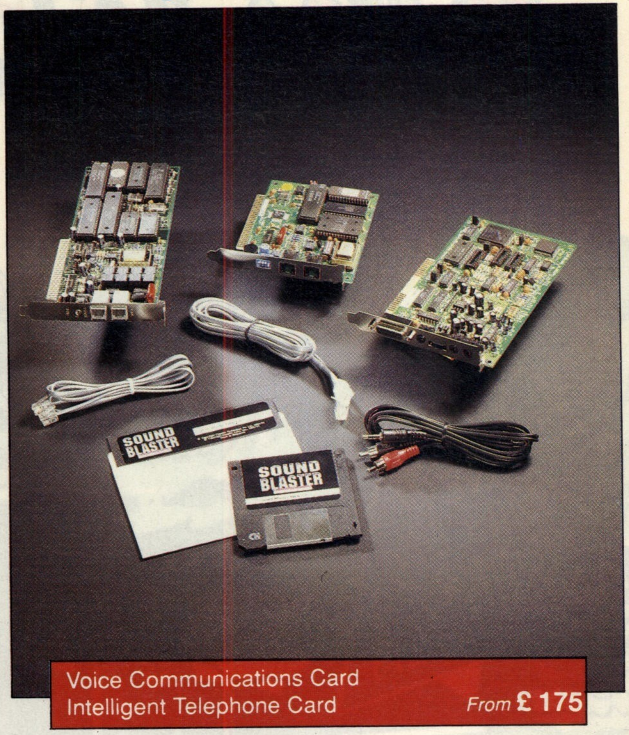

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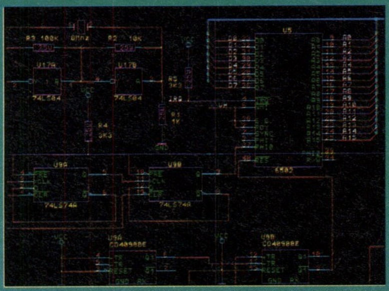

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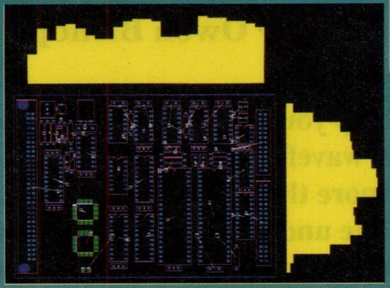

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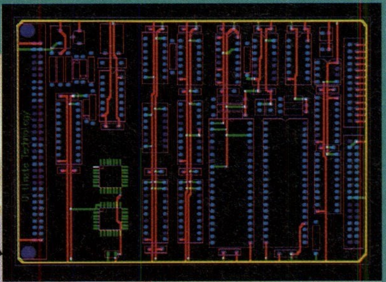

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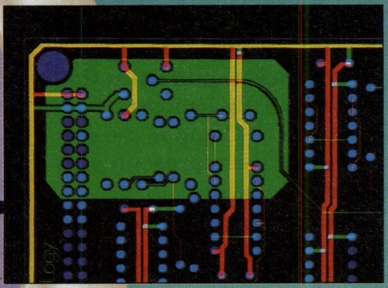

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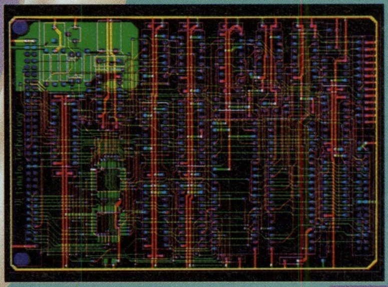

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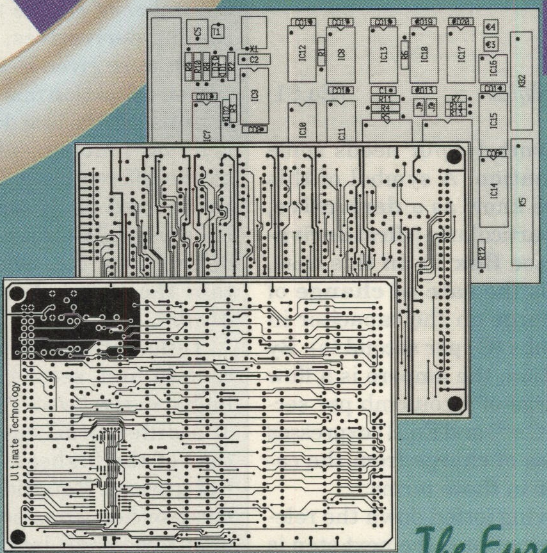

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FIGURING IT OUT

PART 12 – BUILDING MODELS

By Owen Bishop

This series is intended to help you with the quantitative aspects of electronic design: predicting currents, voltage, waveforms, and other aspects of the behaviour of circuits. Our aim is to provide more than just a collection of rule-of-thumb formulas. We will explain the underlying electronic theory and, whenever appropriate, render some insights into the mathematics involved.

Figure 103 shows a very simple circuit. The capacitor is previously charged to 9 V by an external source. The source is removed, current i flows through the resistor, and the pd across the capacitor gradually falls. We are asked to calculate how long it takes for the current to fall to 100 µA.

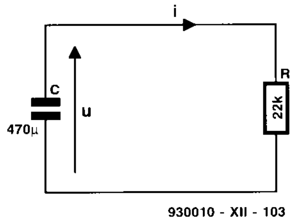

Fig. 103

One way to answer this question is to set up the circuit, including a microammeter to measure i, and measure the time with a stop-watch. Timing is not the difficulty; discharging takes several tens of seconds. The problem is to find a capacitor of exactly 470 µF. We are driven to another way of answering the question – writing an equation which behaves in exactly the same way as the theoretical circuit. Such an equation is a **model** of the circuit.

Modelling

It is easy to find the current at the instant the external source is removed. At that instant, we have a pd of 9 V across a 22 kΩ resistor and

$$i = 9/22\times10^3 = 409\ \mu\text{A}.$$

But, as soon as that current starts to flow, the charge on the capacitor is reduced, causing the pd across it to be reduced, too. The effect of this is that the current is reduced. It decreases from 490 µA, falling eventually to zero (at least, in practical terms: theoretically, it **never** reaches zero). This circuit is one in which key quantities are changing in time. This is the reason for using the lower-case symbols i and u; they are to indicate quantities that vary in time. By contrast, quantities such as C and R are constant and are represented by capital letters.

The first step of building a model of the circuit is to write equations to express all the relationships we know. For this circuit, we know that

$$q = uC \qquad \text{[Eq. 79]}$$

where q is the charge on the capacitor **at any instant**. We also know that

$$u = iR \quad \text{(Ohm's law)[Eq. 80]}$$

and

$$i = \mathrm{d}q/\mathrm{d}t \qquad \text{[Eq.81]}$$

The symbol $\mathrm{d}q/\mathrm{d}t$ needs some explanation. A symbol of this form is know as a **derivative**, more particularly, a **first derivative** (see **Box 1**). In this case, $\mathrm{d}q/\mathrm{d}t$ is the **rate of change** of the charge on the capacitor in coulombs (C) per second (s). By definition, the ampere is a flow of charge of 1 coulomb per second ($1\ \mathrm{C\,s^{-1}}$) and Eq. 81 expresses the loss of charge from the capacitor in these terms.

Having jotted down the relevant equations, the next step is to relate q and $\mathrm{d}q/\mathrm{d}t$ in a single equation. Combining Eq. 79 and 80 gives:

$$q = uC = iRC \qquad \text{[Eq. 82]}$$

Combining Eq. 81 and 82:

$$q = iRC = \mathrm{d}q/\mathrm{d}t\times RC$$

$$\therefore\ \mathrm{d}q/\mathrm{d}t = -q\,/\,RC \qquad \text{[Eq. 83]}$$

Equation 83 is a model of the circuit, relating the instantaneous current (represented by $\mathrm{d}q/\mathrm{d}t$) to the instantaneous charge, with R and C as constants. The negative sign indicates that the charge is decreasing with time. Readers will recognize the divisor RC as the **time constant** (τ) of the circuit.

Because it contains a derivative or differential, Eq. 83 is know as a **differential equation**. The differential terms in such an equation express rates of change, so such equations are widely used a models for dynamic systems. They are ideal for modelling elec-

Derivatives

Given that y is a function of x (for example, $y = 4 + 3x$), the symbol $\mathrm{d}y/\mathrm{d}x$ stands for the **first derivative** of y with respect to x. It is the **rate of change** of y with respect to x. If we think of a graph in which y is plotted against x, $\mathrm{d}y/\mathrm{d}x$ is the gradient of the graph at any point. Finding the derivative (sometimes called the **differential**) of a function is known as **differentiation**. There are a number of simple rules for finding derivatives, some of which were given in Part 5.

When a function has been differentiated, the first derivative is a new function, which can also be differentiated. This gives the **second derivative**, symbol $\mathrm{d}^2y/\mathrm{d}x^2$. We can go on and differentiate this again to obtain the **third derivative**, $\mathrm{d}^3y/\mathrm{d}x^3$, and so on.

Differential equations may contain first, second, third or higher derivatives. The **order** of a differential equation is that of the highest differential present. Equation 83 is a **first-order** equation. Next month we shall look at some second-order equations.

Box 1

Solving the growth/decay equation

Equation 83 is a typical example of the decay equation. It specifies the rate at which the charge diminishes or decays. With a positive coefficient on the right of the equation, it specifies growth.

Given a differential equation, it may be possible to write it in the form

$$\mathrm{d}y/\mathrm{d}x = ky.$$

Note that the right-hand side consists of only a single term in y (no x, no y^2, and so on). Also, k must be a constant, but may be positive (growth) or negative (decay). In Eq. 83, $k = -1/RC$. The solution of such an equation is:

$$y = Ae^{kx},$$

where A is an arbitrary constant. The value of A may be calculated if a set of border conditions is specified (see main text).

Box 2

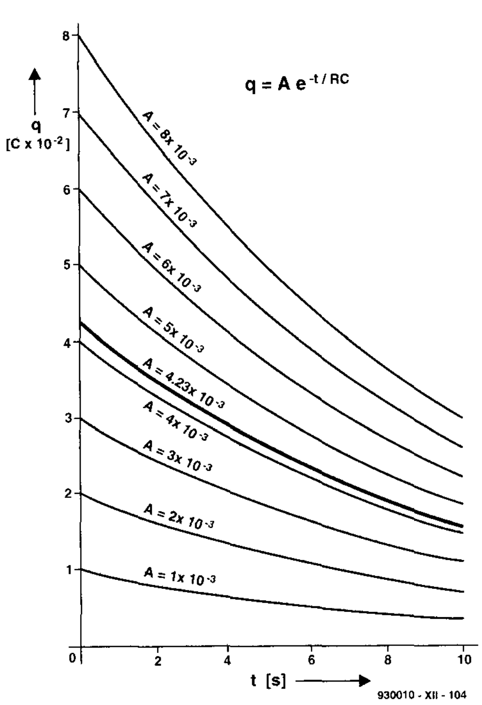

Fig. 104

tronic circuits, and we shall use them to build several models, this month and next.

Solving the equation

The next step is to solve the differential equation. We need to be able to find the value of q at any given time t. Having found q, we can easily find what u and i are at that time. There is no space to go into the steps of solving Eq. 83, but applying the rules quoted in **Box 2** gives us the solution:

$$q = Ae^{-t/RC} \qquad \text{[Eq. 84]}$$

For such a simple circuit, this appears to be rather a complicated solution but, when looked at analytically, it makes sense. We will defer the original task of finding the current until we have examined in more detail the way in which q varies with t. At present, we have what is called the **general solution** to Eq. 83. We need to find the **particular solution** which relates to the values and conditions of our circuit.

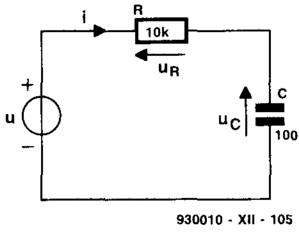

Fig. 105

The key symbol in Eq. 84 is e, the exponential constant. This has a negative index, showing that q is decreasing with time. The index is proportional to t, but has R and C as divisors to take into account the effects of substituting different capacitors and resistors in the circuit. With the values given in **Fig. 103**:

$$q = Ae^{-0.0967t} \qquad \text{[Eq. 85]}$$

The quantity A, known as the **arbitrary constant**, is the next to be determined. This constant is there because the technique for solving Eq. 83 produces an infinitely large number of general solutions, depending on the the value we allot to A. **Figure 104** shows just 10 of the possibilities. Which one of these represents the circuit in our problem?

Border conditions

If the values R and C were all that were known, we could not find A. Any of the curves in **Fig. 104**, or any of many others not drawn there, fits the differential equation. But we also know that the capacitor is charged to 9 V when $t = 0$. These two values specify the **border conditions**. When $t = 0$, $C = 470\,\mu\text{F}$ and $u = 9$ V, by substitution in Eq. 79:

$$q = uC = 9{\times}470{\times}10^{-6}$$

$$= 4.23{\times}10^{-3}\ \text{C}$$

Substituting $q = 4.23{\times}10^{-3}$ C and $t = 0$ in Eq. 84, the index of e becomes zero:

$$4.23{\times}10^{-3} = Ae^{0} = A.$$

We now have a value for A to put in Eq. 84:

$$q = 4.23e^{-0.0967t}{\times}10^{-3} \qquad \text{[Eq. 86]}$$

This is a particular solution of Eq. 83. Its graph is the curve drawn as a heavy line in **Fig. 104**, and shows how the charge on the capacitor falls with time at an ever-decreasing rate.

Knowing the instantaneous value of q at any time, we can calculate u and i at the same instant. From Eq. 79 and 80:

$$i = u/R = q/RC.$$

From Eq. 86:

$$i = (4.23e^{-0.0967t}{\times}10^{-3})/RC$$

$$= (4.23e^{-0.0967t}{\times}10^{-3})/10.34$$

$$\therefore\ = 409.1e^{-0.0967}{\times}10^{-6}.$$

We could plot a curve for i against t, and this would have a similar form to the curve for **Fig. 86**. In this problem, we want to know t when $i = 100\,\mu$A. Substituting $i = 100{\times}10^{-6} = 10^{-4}$:

$$0.2444 = e^{-0.0967t}.$$

Taking natural logarithms:

$$\ln 0.2444 = -0.0967t$$

$$-1.4088 = -0.0967t$$

$$\therefore\ t = 14.57,$$

that is, the current falls to 100 µA after 14.57 s.

Falling pd

Consider the same circuit but with $C = 220\,\mu$F and $R = 100\,\text{k}\Omega$. The capacitor is charged, then allowed to discharge for 10 s, after which time the pd across it is 2 V. Find the initial pd and the pd after 15 s.

The differential equation is Eq. 83, and the general solution is Eq. 84 as above. The border conditions are that $u = 2$ V when $t = 2$ s.

When $u = 2$, $uC = 2{\times}220{\times}10^{-6} = 440{\times}10^{-6}$. In Eq. 84, the index of e is $-10/RC = -0.4545$. Substituting in Eq. 84:

$$440{\times}10^{-6} = Ae^{-0.4545}$$

$$= A{\times}0.6348,$$

$$\therefore\ A = (440{\times}10^{-6})/0.6348$$

$$= 6.931{\times}10^{-4}.$$

Having used the border conditions to find the arbitrary constant A, find the initial charge by putting $t = 0$ in Eq. 84:

$$q = A = 6.931{\times}10^{-4}.$$

This gives the initial pd:

$$u = q/C$$

$$= (6.931{\times}10^{-4})/(220{\times}10^{-6})$$

$$= 3.15\ \text{V}.$$

The pd after 15 s is found in a similar way. The index of e is $-15/RC = -0.6818$.

$$q = 6.931{\times}10^{-4}{\times}e^{-0.6818}$$

$$= 3.505{\times}10^{-4}.$$

$$u = (3.505{\times}10^{-4})/(220{\times}10^{-6})$$

$$= 1.59\ \text{V}.$$

First-order equations

A first-order differential equation has the form:

$$dy/dx + f(x)y = g(x).$$

Both $f(x)$ and $g(x)$ are functions of x, but one or both may be constants or zero, thus simplifying the equation.

An equation such as this is needed for modelling the circuit of **Fig. 105**. Here the capacitor is being charged through a resistor by a variable pd, u. As before, we write down relevant equations:

$$u_R = Ri = R{\cdot}dq/dt;$$

$$u_C = q/C.$$

We can relate these by making use of the fact that, at any instant, KVL applies:

$$u = u_R + u_C$$

$$\therefore\ u = R{\cdot}dq/dt + q/C.$$

Rearranging terms and dividing by R to give dq/dt unity as its coefficient:

$$dq/dt + q/RC = u/R. \qquad \text{[Eq. 87]}$$

This is the first-order equation

that models the circuit.

The equation may be solved by the routine summarized in **Box 3**. This involves calculating a quantity known as the **integration factor**, the purpose of which is to produce an equation that is easy to simplify later. The routine requires integration: some of the procedures for this were outlined in Part 5.

We identify the function $f(t)$ as the constant $1/RC$ and $g(t)$ as u/R.

$F(t) = \int 1/RC \, \mathrm{d}t = t/RC$. The integration factor is $\mathrm{e}^{t/RC}$.

$$G(t) = \int (u/R)\,\mathrm{e}^{t/RC}.$$

If we assume that u is a constant, the integration is simpler. We will now refer to it as U.

$$G(t) = RC\,[(U/R)\,\mathrm{e}^{t/RC}]$$

$$= CUe^{t/RC}.$$

The solution is:

$$q = -\mathrm{e}^{-t/RC}.CU\mathrm{e}^{t/RC} + \mathrm{Ae}^{-t/RC}.$$

In the first term on the right, the indices of e total zero, and $\mathrm{e}^0 = 1$:

$$q = CU + \mathrm{Ae}^{-t/RC} \qquad \text{[Eq. 88]}$$

This is the general solution. If the capacitor has zero charge when $t = 0$, we have a border condition:

$$0 = CU + \mathrm{A},$$

$$\therefore\ \mathrm{A} = -CU.$$

Equation 88 becomes:

$$q = CU(1-\mathrm{e}^{-t/RC}) \qquad \text{[Eq. 89]}$$

This is the particular solution, assuming that the source is switched on at $t = 0$ and holds a constant value U. **Figure 106** shows the curve for this equation if $U = 6$. The charge on the capacitor rises rapidly at first, but at a gradually decreasing rate until it almost, but never quite, reaches CU.

Charging times

A related equation is obtained by dividing Eq. 89 throughout by C. The pd across the capacitor is q/C, which we will refer to as u_C. Then, dividing:

$$u_C = U(1-\mathrm{e}^{-t/RC})$$

$$\therefore\ u_C/U = 1-\mathrm{e}^{-t/RC}. \qquad \text{[Eq. 90]}$$

Equation 90 can be used to determine the time to reach any given pd u_C expressed as a fraction of the applied pd U. In the standard 555 timer circuit, the monostable period is the time taken for the pd across the capacitor to rise from $U/3$ to $2U/3$, where U is the supply voltage.

$u_C/U = 1/3$ at t_1:

$$1/3 = 1-\mathrm{e}^{-t_1/RC}$$

$$-2/3 = -\mathrm{e}^{-t_1/RC}.$$

Negating and taking logarithms:

$$\ln(2/3) = -t_1/RC$$

$$t_1 = 0.4055RC.$$

$u_C/U = 2/3$; at t_2:

$$2/3 = 1-\mathrm{e}^{-t_2/RC};$$

$$1/3 = -\mathrm{e}^{-t_2/RC};$$

$$\ln(1/3) = -t_2/RC;$$

$$t_2 = 1.0986RC.$$

The monostable period is t_2-t_1 $=(1.0986-0.4055)RC = 0.6931RC$. This is the period quoted in the data sheet for this timer.

Inductors

The derivative which models the action of an inductor is:

$$u = L{\cdot}\mathrm{d}i/\mathrm{d}t.$$

The induced e.m.f., u, is proportional to the inductance L and the rate of change of current, i. For the circuit of **Fig. 107**, the equations are:

$$u_R = Ri;$$

$$u_L = L{\cdot}\mathrm{d}i/\mathrm{d}t.$$

By KVL:

$$u = u_R + u_L = Ri + L{\cdot}\mathrm{d}i/\mathrm{d}t.$$

Rearranging terms and dividing throughout by L gives the differential equation:

$$\mathrm{d}i/\mathrm{d}t + (R/L)i = u/L.$$

Applying the rules for solving first-order equations, we have:

$$f(t) = R/L;$$

$$\therefore\ F(t) = Rt/L.$$

Integrating factor is $\mathrm{e}^{Rt/L}$.

$$g(t) = u/L;$$

$$\therefore\ G(t) = \int (u/L)\,\mathrm{e}^{Rt/L}\,\mathrm{d}t.$$

We make simplifying assumptions in a moment. Here is the solution at this stage:

$$i = \mathrm{e}^{-Rt/L}\int (u/L)\,\mathrm{e}^{Rt/L}\,\mathrm{d}t + {}$$
$$+ \mathrm{Ae}^{-Rt/L}.$$

Note that the index of e is sometimes + and sometimes –. If u is a function of t, for example, u is an alternating pd with a function such as $u = 2\sin\omega t$, we integrate the first expression on the right, and obtain a particular solution. Here we assume that u is constant and call it U. Integrating the term gives:

$$\mathrm{e}^{-Rt/L}\,(U/L){\cdot}\mathrm{e}^{Rt/L}\,(L/R)$$
$$= u/R.$$

Now the solution is simplified to:

$$i = U/R + \mathrm{Ae}^{-Rt/L}. \qquad \text{[Eq. 91]}$$

For the particular solution, take the case in which the pd is 10 V up to the time $t = 0$. The current is steady ($\mathrm{d}i/\mathrm{d}t = 0$), being determined only by the pd and the resistor:

$$i = 10/(220\times10^3) = 45.45\times10^{-6}.$$

Substituting in Eq. 91:

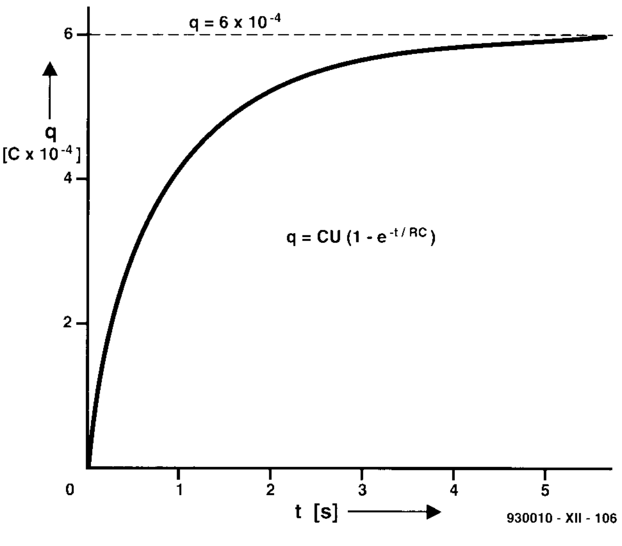

Fig. 106

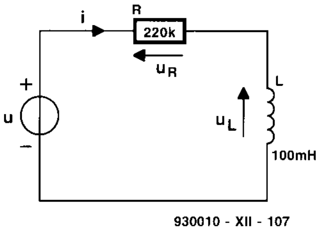

Fig. 107

Solving first-order equations

Given an equation in the form $\mathrm{d}y/\mathrm{d}x + f(x) + g(x)$.

1. Integrate $\int f(x)\,\mathrm{d}x$ and call it $F(x)$.
2. The integrating factor is $\mathrm{e}^{F(x)}$.
3. Integrate $\int g(x)\,\mathrm{e}^{F(x)}\,\mathrm{d}x$ and call it $G(x)$.
4. The solution is: $y = \mathrm{e}^{-F(x)}\,G(x) + \mathrm{Ae}^{-F(x)}$.

Note the negative indices at stage 4. A is the arbitrary constant; find it by using boundary conditions.

Box 3

Integration

Integrating a constant, $1/RC$: Table 1, Part 2, states that the integral of $t^n = t^{n+1}/(n+1)$, provided that $n \neq -1$. Since t does not appear in the expression being integrated, $n = 0$. The integral of t^0 is t. Multiplied by the constant $1/RC$, the integral of $1/RC$ is t/RC.

Integrating $\mathrm{e}^{t/RC}$: Table 1 in Part 2 states that the integral of e^{at} is e^{at}/a. Here, $a = 1/RC$. The integral is

$$(\mathrm{e}^{t/RC})/(1/RC) = RC\mathrm{e}^{t/RC}.$$

Box 4

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$$A = 45.45\times10^{-6} - U/R.$$

Putting this value of A into Eq. 91, we have the particular solution:

$$i = U/R + (45.45\times10^{-6} - U/R)\,e^{-Rt/L} \qquad \text{[Eq. 92]}$$

When $t = 0$, the applied pd is 10 V and we have a constant current of 45.45 μA flowing through the circuit. The voltage source is suddenly reduced to 0 V. To find what happens, insert $U = 0$ in Eq. 92:

$$i = 0/R + (45.45\times10^{-6} - 0/R)\,e^{-Rt/L};$$

$$\therefore\ i = 45.45\times10^{-6}\times e^{-Rt/L}. \qquad \text{[Eq. 93]}$$

Figure 108 is the graph of this. It shows the current gradually dying away at a rate depending on the inductance and resistance.

We can also investigate what occurs if the voltage is reduced not to zero, but to a lower voltage, say, 5 V:

$$i = 5/R + (45.45\times10^{-6} - 5/R)\times e^{-Rt/L}.$$

Or we can model a suddenly increased voltage to, say, 22 V:

$$i = 22/R + (45.45\times10^{-6} - 22/R)\times e^{-Rt/L}.$$

Figure 109 shows the graphs, which clearly reflect the action of an inductor in resisting changes in the flow of current through it. We could also modify Eq. 93 by changing the value of L and seeing what effect this has on the extent and timing of current changes.

Once a model has been built mathematically, it is easy to insert new values and determine its behaviour. This is much easier than building a circuit, then replacing resistors, capacitors or inductors. Differential equations are a powerful way of 'figuring it out'.

Next month we shall model more complicated circuits with second-order equations.

Test yourself

1. Write the particular solution *for the current in the circuit* of **Fig. 103**, but with $C = 150\ \mu F$, $R = 4.7\ k\Omega$ and an initial pd of 6 V. Find (a) the pd across the capacitor 1 s after discharge has begun, and (b) the current 2 s after discharge has begun.
2. Find the **rise time** for the circuit of **Fig. 105**, if $U = 10$ V, $C = 10\ \mu F$ and $R = 39\ k\Omega$. Rise time is defined as time for the pd across the capacitor to rise from 10% of U to 90% of U.
3. In the circuit of **Fig. 107**, but with $R = 4.7\ k\Omega$ and $L = 20$ mH, a steady voltage of 1 V is applied until $t = 0$. Then the voltage is changed instantly to 5 V. Calculate the current 2 μs later.

Answers to Test yourself (Part 11)

1. $z_{11} = 6.67\ \Omega$; $z_{21} = 4\ \Omega$; $z_{12} = 4.67\ \Omega$; $z_{22} = 7.47\ \Omega$.
2. $z_{11} = 9.83\ \angle{-5.57°}$; $z_{21} = 1.17\ \angle 77.59°$; gain $= 0.12\ \angle 83.16°$.
3. $h_{11} = 50\ k\Omega$; $h_{21} = 125$; $h_{12} = 1/3$; $h_{22} = 833\ \mu s$.

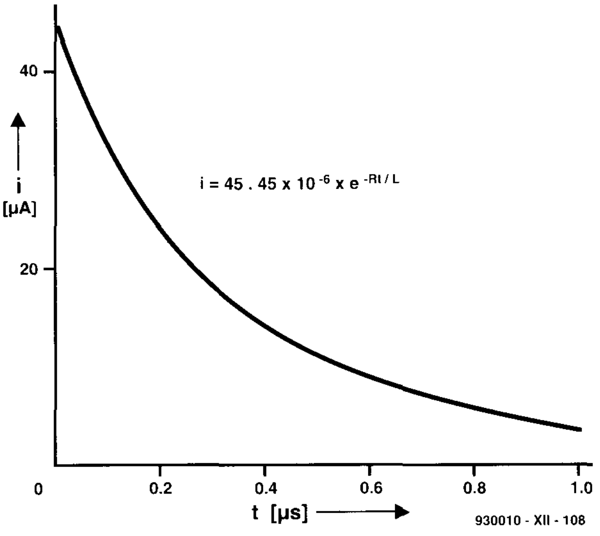


Fig. 108

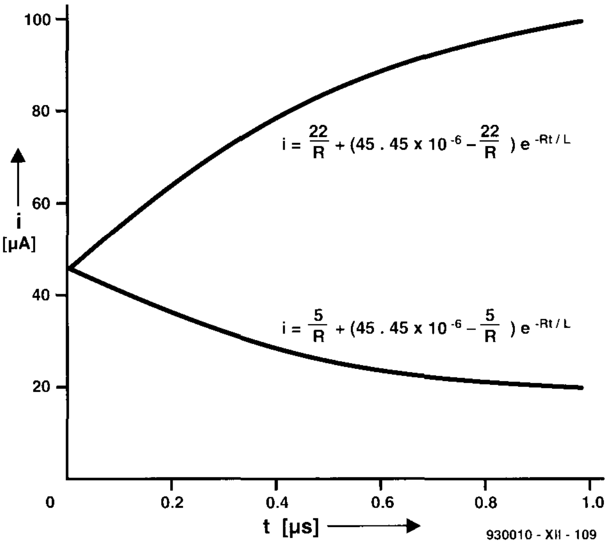


Fig. 109

Coding for GSM

By Brian P. McArdle

1. Introduction

The term GSM stood originally for Groupe Special Mobile. The meaning Global System for Mobile communications has been adopted recently as this is now considered to be a more accurate description. It is the new form of cellular telephone system intended to replace the present TACS. The purpose of this article is to review the coding methods for voice and data.

The GSM projects was commenced in 1982 by CEPT in order to design a pan-European cellular telephone system which could be operated throughout western countries. It was not the first cellular network as systems, such as TACS, were already in operation by a number of administrations. However, these other systems tended to be confined and mobile units could not be used outside their own countries. Since international travel, especially between countries of the EC, had become commonplace, a clear requirement existed for a pan-European system. There was the added advantage that one system would reduce the difficulties of manufacturers who were attempting to cater for the specifications of different national systems. The EC wished to eliminate barriers to trade between member states and, consequently, the concept of just one system fitted in with these policies.

The TACS system uses narrowband frequency modulation (NBFM) for voice communication. The frequency range is 935–960 MHz for base stations and 890–915 MHz for mobile units. During a call, the mobile transmits on a specific channel and receives from the base on another dedicated channel simultaneously. The frequency separation between the two ranges permits duplex operation. In both ranges, the channel spacing is 25 kHz. The frequency deviation at 9.5 kHz is unusually high, but frequencies are assigned to avoid interference between adjacent channels. However, the system differs from business radio in that specific channels are not assigned to individual users. Unknown to users, base and mobile stations exchange control signals on control channels that are reserved for this purpose and are not used for voice communications. A roaming mobile monitors the base control channels and selects the strongest signal. It identifies itself to the selected base on a mobile control channel in order to ensure that all appropriate calls are routed to that particular base. If the mobile moves away into another cell where a different base has a stronger signal, the procedure is repeated. While the voice channels use frequency modulation, the control signals are transmitted using digital modulation (PSK – phase-shift keying) at 8 kbits/second. Some control signals are sent over the voice channels but, in general, the two operate separately.

In GSM, the voice and control channels both use digital modulation. It is an all digital system. The techniques for modulation and coding are examined in sections 2 to 5. The comments expressed are purely personal.

2. Control channels

GSM has two basic types of channel: TRAFFIC for voice and data, and CONTROL. The term LOGICAL is sometimes applied. Both types use burst transmissions and Time Division Multiplexing (TDM) as required. Every burst takes a total of 577 microseconds. A PHYSICAL channel means a sequence of such time slots for communication of a full message between base and mobile stations. This is not a radio-frequency channel as the frequency can be altered. A frame is a prescribed sequence of eight bursts where a caller is assigned to one in every eight slots. Thus, eight callers are multiplexed together with respect to time. These points are further explained in Sections 3 and 4. For operation of a GSM unit, a user is not aware of the complicated signalling procedures for implementation.

A control channel can be broadcast (3), common (3) or dedicated (8). The functions are not examined in this article as the emphasis is on coding. Each channel can have more than one application. It could contain a combination of frequency correction, synchronization and broadcast information (e.g., for base station identification). For example, a synchronization burst (148 bits) is transmitted by a base on the Broadcast Synchronization Channel with the format

Tail bits (3)	Encrypted bits (39)	Synchronization sequence (64)	Encrypted bits (39)	Tail bits (3)	Guard period (8.25)

◄ 577 microseconds ►

◄ 156.25 bit periods ►

Tail bits can be taken as ‘0’ unless otherwise stated. The guard period is to permit a unit to power down on termination of a burst. The first six bits after the tail bits represent the base's identifier and so on. The term‘encrypted bits’ refers to the information bits that are encrypted (Appendix 1) before modulation and transmission. Alternatively, an access burst (88) is transmitted on a Common Control Channel as follows

Tail bits (8)	Synchronization sequence (41)	Encrypted bits (36)	Tail bits (3)	Guard period (68.25)

In this particular case the tail bits are extended to length 8: 00111010 and the 41 synchronization bits are also specified. It should be noted that the various signals do not contain the same number of useful bits, but the total duration remains constant.

An interesting point is that frequency hopping is in use. It is implemented on mobiles. However, this is not the spread spectrum form where a radiofrequency signal is deliberately spread across a bandwidth much larger than required for a message. In true spread spectrum the bandwidth is independent of a message, but is determined by a prescribed modulating signal. In GSM, the channel does not remain the same for the duration of a message. Unknown to a user, the channel changes automatically on receipt of a specific signal. The hopping occurs between the time slots when a mobile is not transmitting. The main purpose of hopping is to maintain the maximum possible level of spectrum efficiency. However, the fact that a full message is transmitted on a number of channels helps to minimize the effect of a poor channel (e.g., due to a high noise level or an interfering signal).

The control signals undergo encoding procedures similar, but not identical, to those for voice and data. These are discussed in the next two sections.

3. Voice communications

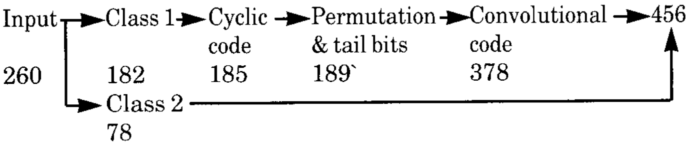
GSM is an all digital system, which means that the speech signals must be digitized. At present, there is one speech codec, known as RPE-LTP, in use. Another codex, which would reduce the number of bits by half, is still under development.

The full rate codex uses Linear Predicitive Coding (Appendix 3). It suffices to state that the codex is a good representation of human speech. The analogue audio signal is sampled every 20 milliseconds and a block of 260 bits is formed as follows

Class 1 (182)	Class 2 (78)
$d_0\, d_1\, d_2 \ldots d_{181}$	$d_{182}\, d_{183}\, d_{184} \ldots d_{259}$

where d_0 and d_{259} are the MSB and LSB respectively. Class 1 is particularly important and undergoes a series of encoding operations.

Class 2 remains unprotected. An analysis of the method of selection of each class is not necessary to understand the coding procedure. Both classes eventually form a new block which is input to the encryption unit (Appendix 1). The various steps can be summarized as follows



The cyclic encoder uses a generator polynomial ($x^3 + x + 1$) to deduce three check bits from the polynomial ($d_0x^{52} + d_1^{51} + \ldots d_{49}x^3 + c_0x^2 + c_1x + c_2$). The check bits are chosen such that the residue polynomial is ($x^2 + x + 1$). Refer to Appendix 5 for the mathematical background. If an error occurs in just one bit, there is a total of 53 possibilities. However, the check bits are limited to a total of eight possible combinations, including the case for no error. Obviously, further operations are required for an adequate level of protection. The new block is reordered according to

0 1 … 90	91 92 93	94 95 … 184	185 186 187 188
d_0 d_2 … d_{180}	c_0 c_1 c_2	d_{181} d_{179} … d_1	
u_0 u_1 … u_{90}	u_{91} u_{92} u_{93}	u_{94} u_{95} … u_{184}	0 0 0 0

The even-numbered data bits from 0 to 180 are placed in the first 91 positions. The odd-numbered bits are in the last 91 locations in reverse order before the tail bits which are set to '0'. The convolutional encoder generates a new block according to the equations

$$v_{2n} = (u_n + u_{n-3} + u_{n-4}) \bmod 2$$
$$v_{2n+1} = (u_n + u_{n-1} + u_{n-3} + u_{n-4}) \bmod 2$$

for n = 0 to 188 and the block size is doubled. Class 2 bits are placed in positions 378 to 455. At this point, a fundamental data block is fully constructed. The blocks are interleaved by reordering and scattering the bits over a total of eight blocks. Transmission of a NORMAL BURST is of the form

Tail	Data	Flag 1	Training	Flag 2	Data	Tail	Guard
3	57	1	sequence 26	1	57	3	8.25
	encrypted			encrypted			

The effect of interleaving is that 57 bits are from the original block and the remaining 57 are from the next block. A training sequence is included between the useful information bits. This takes part in the modulation, but not in the encryption process and need not be considered further. Two flags are added for control purposes since control signals are sometimes transmitted on traffic channels. As per Section 2, GSM has very extensive signalling requirements and, consequently, traffic signals must double up as control channels when the deignated control channels have insufficient space for additional signals. For voice or data (Section 4), both flags are set to '0'. If flag 1 or 2 is set to '1', then the even or odd numbered bits respectively carry control information. Hence, the term 'stealing flags' is applied. A full block of 456 bits has eight flags added to produce a final size of 464.

GSM makes extensive use of Time Division Multiplexing. Successive bursts, as per the previous NORMAL BURST, are not from the same caller. A traffic channel contains eight different callers in successive time slots and a slot corresponds to a burst. Each caller has one in every eight slots.

The reader is referred to ETSI Specification I-ETS 300 031 for an exact description. The speech codec is an improvement on ADPCM (Appendix 2) which is widely used for digital communications. Decoding procedures are not analysed as they are left to the manufacturers. This is in line with normal practice of late. Most decoding algorithms will probably be based on the syndrome method. A previous article in this magazine[7] has some relevant examples on the above convolutional code.

GSM offers a major improvement in the level of confidentiality, even without encryption, due to the complicated signalling arrangements, frequency hopping and multiplexing of messages. Low-cost equipment, which can monitor the TACS system on NBFM, is useless against GSM. Even with the speech codec and decoders installed, a scanner would still have to be capable of identifying the appropriate control signals and a particular burst among a total of eight over a complete cycle in order to eavesdrop on a particular conversation. It is quite likely that test and monitoring equipment will become so sophisticated that it could be designed and made only by the GSM manufacturers.

4. Data communications

GSM is not limited to speech, but has the facility to transmit data at the following rates:

(a) full rate at 9.6 kbits/second
(b) full rate at 4.8 kbits/second
(c) full rate at 2.4 kbits/second
(d) half rate at 4.8 kbits/second
(e) half rate at 2.4 kbits/second.

Since the coding procedures are very similar, the analysis is confined to (a) and (b).

For (a), the information is input as 60 bits every five milliseconds. Four blocks are chained together to generate a 240 bit block which is processed as follows:

Input →	4 blocks →	Tail bits →	Convolutional code →	Reduction to 456
60	240	244	488	456

The convolutional code uses the same two equations as in Section 3 to double the block size. The bits in locations 11 to 42 are removed to produce a reduced block of 456. This block is interleaved such that the bits are distributed over 19 blocks. Transmissions are in the format of a NORMAL BURST.

For (b), the input is 60 bits every 10 milliseconds. The procedure is:

Input →	Tail bits →	2 blocks →	Convolutional code →	Interleaving
60	76	152	456	

The tail bits are included within the 76 bit block as follows:

Data	Tail	Data	Tail	Data	Tail	Data	Tail
d_0–d_{14}	bits	d_{15}–d_{29}	bits	d_{30}–d_{44}	bits	d_{45}–d_{59}	bits
15	4	15	4	15	4	15	4

$u_0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots u_{75}$

Another block is generated as per above and entered into positions 76 to 151. A convolutional code trebles the block to 456:

$$v_{3n} = (u_n + u_{n-1} + u_{n-3} + u_{n-4}) \bmod 2$$
$$v_{3n+1} = (u_n + u_{n-2} + u_{n-4}) \bmod 2$$
$$v_{3n+2} = (u_n + u_{n-1} + u_{n-2} + u_{n-3} + u_{n-4}) \bmod 2$$

and is interleaved, encrypted and transmitted in the format of a NORMAL BURST. A simplified decoding method is demonstrated in Appendix 6.

For voice and data, the encryption operation occurs after the other encoding operations and just before the modulation process. This is not the standard configuration. Generally, error control encoders are the last step before modulation and transmission. The arrangement suggests some form of stream encryption where an error in transmission has no effect on the decryption operation. An error in one bit remains a single error which can be corrected by the convolutional code. (In block encryption, a single error could affect an entire block.) It also indicates that the radiofrequency signals should be transmitted on reliable interference-free channels. Frequency hopping (Section 2) should be of assistance in maintaining communications.

5. Modulation

The method of modulation is Gaussian Minimum Shift Keying (GMSK). The term 'Gaussian' refers to the shape of the modulating waveform. After the encryption unit, the bits are sent to the modulator for digital modulation of a radio frequency carrier. In order to indicate start and stop positions in the process, the modulator has the facility to add dummy bits to the stream of data bits. This consists of a sequence of 1s before and after the data burst and the modulator behaves as if these dummy bits are input in the standard manner. For electronic implementation, the bits are turned into bipolar form (1 and –1) as per the following equations and filtered to generate the modulating signal.

$$q_n = (p_n + p_{n-1}) \bmod 2.$$

$$s_n = 1 - 2q_n.$$

The last equation represents a differential operation since s_n becomes the difference between the current bit at stage n and the previous bit. In electronic terms, the s_n s are Dirac pulses which are input to a filter with very specific characteristics. Its response is designed to generate pulses with a Gaussian shape which, in turn, are used to phase-modulate a radiofrequency carrier. The transmitted signal in the **time domain** is of the form

$$x(t) = \sqrt{(2E/T)} \cos[\omega t + \theta(t) + \theta_0]$$

where θ represents a random phase shift and can be assumed to be constant for the duration of a burst. The modulation is $\theta(t)$ and produces a phase shift and side bands in the unmodulated carrier. The other terms are

E = energy per modulation bit
ω = angular frequency of the carrier
T = duration of one bit
$BT = 0.3$ where B = 3 dB bandwidth.

The maximum phase shift per modulation bit is 90° and the modulating index is less than 0.5. Hence, the term 'minimum' reflects the electronics restrictions of the modulation process. The effect is that the radio frequency spectrum is compressed in comparison with the older techniques of angle modulation (frequency and phase modulation). For example, the first sidelobe is 23 dB below the level of the main transmission, whereas in PM this figure is 13 dB. Obviously, there must be a high level of precision in the interpretation of phase changes. In the specification for radio transmission and reception, there is a requirement for phase accuracy. A burst in the process is 156.25 bit durations and the modulation rate is 270.83 kbits/second. The reader is referred to ETSI Specification I-ETS 300 032 for a detailed analysis.

6. Radio frequency characteristics

GSM has two bands for dual frequency operation. A base station transmits on one of the 124 channels in the range 935–960 MHz and receives on another channel in the range 890–915 MHz. For mobile operation, these two bands are reversed. To safeguard other services in adjacent bands, channels 1 and 124 are normally not used. In each band the channel spacing is 200 kHz with eight separate messages, either voice or data, multiplexed on to the same channel as per Sections 2 and 3. Each frame of a message is allocated a time slot of 577 microseconds for transmission of 156.25 bits. The transmission rate is so fast that adjacent channels cannot be operated within the same general area (e.g., between adjacent cells). It is recommended that a separation of at least 400 kHz be applied.

Due to the high frequency range, the transmitted signals are propagated from base to mobile and vice versa by multipath rather than directly. They arrive in the general area of a mobile with random variations in level and different delays. In the immediate vicinity of a mobile there are further variations mcaused by local reflections, diffractions and the arrival angle. Over distances of around 10 metres, the criterion for a wide-sense stationary process is satisfied. For test purposes, propagation models have been developed for different environments: urban, rural, and hilly terrain, but are outside the scope of this paper. It suffices to state that special difficulties are encountered for high bit rates at high frequencies and the GSM system has been designed to cope with these problems. The frequency hopping mechanism (Section 3) is an attempt to maximize the chances of reliable communications by moving a user through successive electronic channels during a full message.

There are various classes of units for different applications. Base stations are available in eight ranges from 2.5 watts to 320 watts. There are five classes of mobile from 0.8 watts to 20 watts. Some are fitted with an integral antenna and others have a socket for connection to an external antenna. In transmit mode, the ouput spectrum is determined by two main effects: modulation process owing to the use of burst type modulating signals and switching transients due to frequency hopping. For the first effect, there is a table of values for various power levels (e.g., an emission at 400 kHz from the nominal transmit frequency should be 58 dB down for a unit with an integral antenna and 60 dB for a unit with an antenna connector). For the second effect, there can be inaccuracies in trying to distinguis between a transient and a spurious emission and, consequently, the two are considered together. The peak transmitted power in specific bandwidths (e.g., 10 kHz, 30 kHz and 100 kHz) at designated frequencies (inside and outside the GSM bands) from the nominal transmit frequency must be within certain limits. A base or mobile in the transmit mode must not emit more than 250 nanowatts at the designated frequencies in the range 9 kHz to 1 GHz. For the range 1 GHz to 12.75 GHz, the level is increased to 1 microwatt. For a mobile in the idle mode, the figures are 2 and 200 nanowatts respectively. Both sets of test are quite complicated and this explanation is only intended to present an overview of the output spectrum of a GSM system.

In general, the radio frequency characteristics are very in volved and the reader is referred to ETSI Specification I-ETS 300 033.

7. Summary

This article only covers the coding aspects of GSM from the point of radio communications. The comments are purely personal and a reader should consult the specifications for the exact position.

Although GSM was originally intended as a pan-European system, it will probably be a number of years before users can transfer automatically between states. Roaming by a mobile as it moves between states was included in the draft, but this could take some years. The proposals were very ambitious, which resulted in complex equipment standards. Introducin g and developing any type of new service, which must be operated on a national scale throughout a country,. will remain a major undertaking. The fact that many states already had cellular systems did not automatically turn GSM into a modification. Despite the difficulties, GSM is an outstanding achievement of design and development for the Europe of tomorrow.

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Appendix 1: Encryption techniques

This article does not examine the method of encryption after the formation of the eight sub-blocks from the 456 bits as per Section 3. However, controversies have arisen over the A5 Encryption Algorithm. There is the difficulty that the encryption and decryption operations have not been published as a specification in the usual manner. The algorithm is restricted to manufacturers and is available only to certain categories of personnel. A few general remarks should provide an overview.

The most widely know encryption algorithm is the US Data Encryption Standard (DES) introduced in 1977 for the encryption of computer data. The input block is 64 bits and, in early applications, was usually constructed from eight ASCII characters of eight bits per character. It is a block cryptosystem operating on groups of bits rather than on individual bits (i.e., stream cryptosystem). The operation is fixed with the exception of a key block of 56 bits. Any combination of bits can be used and, therefore, there are 2^{56} possible keys. The particular key in use is the secret information of the cryptosystem. The key block is sub-divided into 16 separate internal keys, which are applied to the input block in 16 steps to generate the output block of 64 bits. The decryption operation to recover the original block is the same process, but the 16 sub-keys are applied in reverse order. Since the standard is over 16 years old, it is no longer considered suitable for many applications. ETSI is now developing new algorithms for its own particular requirements. However, the DES remains a milestone in the development of modern secrecy systems and has been used as a basis for further designs. It should be around in updated versions until the year 2000.

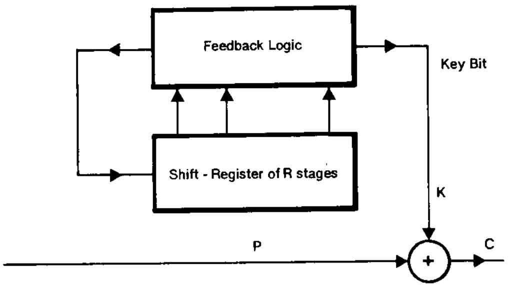

Fig. 1a. Stream encryption system. The method of generating key bits is the secret information and must not be known by an unauthorized user.

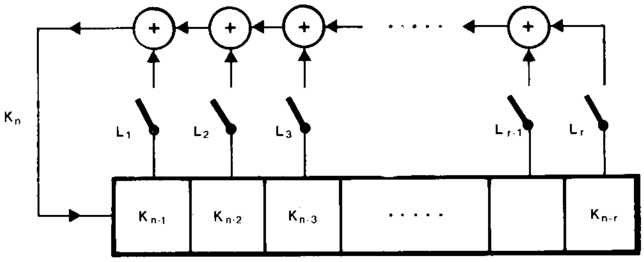

Fig. 1b. Linear feedback shift register. The incoming bit on the left is given by

$$K_n = \sum_{j=1}^{r} L_j K_{n-j} \bmod 2$$

L_j = 1 or 0 for the latch closed or open respectively. Since addition modulo 2 is a linear operation, the feedback logic is the linear variety.

GSM is believed to use sa shift register with non-linear feedback logic similar in principle to that in **Fig. 1**. It does not use a DES type block system. For a shift register of *r* stages (i.e., JK flip-flops) there are

1. 2^{2^r} possible feedback arrangements. If $r = 3$, then $2^3 = 8$ and $2^8 = 256$. The possible sequence of states in the operation of the shift register is

State	: 000	001	010	011	100	101	110	111
Successor 1:	000	000	001	001	010	010	011	011
Successor 2:	100	100	101	101	110	110	111	111.

   Each state has two possible successor as an incoming bit is 1 or 0. In reality, a shift register is designed such that each state has a unique predecessor and successor. This means that each state occurs only once in a complete cycle of states (i.e., period). Thus, the number of different feedback arrangements is reduced to $2^{2^{(r-1)}}$. For $r = 3$, $2^4 = 16$. If the logic required to implement a particular sequence must consist of AND and OR operations, this is known as NON-LINEAR. In mathematical terms, they are represented by non-linear functions.

2. 2^r feedback arrangements with linear logic. The arrangement consists of latches and an EXCLUSIVE-OR operation to represent addition modulo 2. Each flip-flop of the register is connected through a latch, which is open or closed, to the addition operation. Obviously, if a latch is open, the corresponding state of the register has no effect on the generation of an incoming bit. It is the simplest form of feedback logic and the most commonly used by circuit designers. One of the principal applications is in the generation of pseudo-random binary sequences.

3. (2^r-1) linear feedback arrangements which do not generate the state all zeros.

4. $\phi(2^r-1)/r$ linear feedback arrangements which generate maximum length sequences of period (2^r-1). ϕ is Euler's Totient Function.

The main reason for using non-linear logic is security. The techniques of cryptanalysis are considerably more effective against linear than non-linear logic. For example, the encryption operation of **Figure 1** is given by $C = (P + K) \bmod 2$. Since the operation is linear, decryption is given by $P = (C + K) \bmod 2$. In the same manner, K can be deduced from a known pair as follows: $K = (C + P) \bmod 2$ and the secret information has been compromised. This could apply to a full sequence of key bits. It is a general guideline that linearity is the main cryptographic weakness in a system. It is the friend of hackers and the enemy of designers. **Figure 1** is intended to illustrate the overall category and should not be taken as accurate representation of the techniques in GSM.

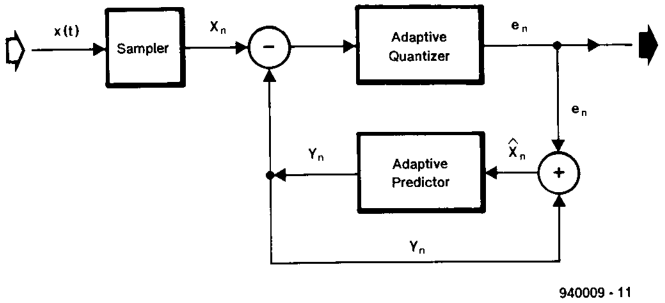

Fig. 2. General arrangement for ADPCM.

Appendix 2: Adaptive differential pulse code modulation (ADPCM)

Figure 2 illustrates the general principles, but is not a detailed circuit. The main point is that the output is not merely a sampled version of the input sequence. The difference between the input and a prediction is quantized to produce another signal. It should be noted that x_n, y_n and e_n are digital numbers and not bits. The output, e_n, will always have at least a quantization error. In non-mathematical terms, the original signal is sampled very often and the difference between each sample and a predicted value of what the sample should be is quantized and transmitted.

The process of prediction is critical for accuracy and depends on the assumption that any two successive samples and their corresponding predicted values do not differ too much. Consequently, the rate of sampling must be sufficiently high for this assumption to remain valid. There can be a major variation over a large number of samples. In fact, the process must be able to handle wide changes as a voice signal can vary substantially in level and frequency. In general, x_n and x_{n-1} should be very similar. Then, if the deduction of y_n by the predictor is accurate, the difference $(x_n - y_n)$ is small. The difference signal is quantized into e_n, which is transmitted. The result is a reduction in the number of bits which would be required to transmit x_n as ordinary PCM.

The simplest form of prediction is based on a recursive filter type operation as follows

$$y_n = \sum_{j=1}^{r} a_j \hat{x}_{n-j}$$

where r is the number of stages in the prediction process and the a_js are the prediction coefficients. y_n is an estimate of x_n as per the previous paragraph and $\hat{x}_{n-j}$ is the reconstructed estimate of the original input at stage $(n-j)$. The coefficients are calculated by a minimization of the Mean Squared Error (MSE). Consider a simplified process where y_n can be replaced by ax_{n-1}.

$$\text{MSE} = \text{E}\,(x_n - y_n)^2 = \text{E}\,(x_n - ax_{n-1})^2$$

$$= \text{E}\,(x_n{}^2) - 2a\text{E}\,(x_n x_{n-1}) + a^2\text{E}\,(x_{n-1}{}^2).$$

$$\text{d/d}a(\text{MSE}) = -2\text{E}(x_n\, x_{n-1}) + 2a\text{E}\,(x_{n-1}{}^2) = 0.$$

The expectations can be replaced by autocorrelation functions deduced from N input samples as follows

$$R(k) = \frac{1}{N}\sum_{j=1}^{N-k} x_j x_{j+k}$$

for $k = 0$ and 1. The same principle can be used for a predictor with a number of stages. Algorithms have been developed to allow automatic calculation. In an adaptive configuration, the values would not be constant.

CCITT Recommendation G.721 gives the process required to turn straight PCM at 64 kbits/second into ADPCM at 32 kbits/second. The adaptive quantizer has 15 levels producing an output block of four bits (three for magnitude and one sign bit) per input. For a sampling rate of 8 kHz, the transmission rate is 32 kbits/second. The quality of speech is only slightly lower than PCM, but the considerable reduction in the number of output bits more than compensates. Recommendation G.722 turns analogue voice in the range 50 Hz to 7 kHz into SB-ADPCM at 64 kbits/second. The frequency band is split into two sub-bands and each is encoded using ADPCM. Further analysis is outside the scope of this paper and is not needed for GSM, which uses Linear Predictive Coding (Appendix 3).

Appendix 3: Linear Predictive Coding (LPC)

This is quite different from ADPCM in that the original signal or a compressed version is not transmitted. The input is sampled and the samples processed as if they had been generated by an all-pole digital filter type operation. In this requirement, LPC is very similar to ADPCM at the input stage. However, the methods differ considerably beyond this point. The main advantage in LPC is that the number of bits required to represent a sample is greatly reduced when compared to PCM. At present, the principal application is in speech codecs.

Figure 3 shows the general technique, but should not be taken as an accurate representation of a very complicated process. In PCM, the signals are analysed in the time domain. However, LPC uses the frequency domain and the output block is primarily a representation of the spectral information of the voice sample. Coarse spectral information is represented as the equivalent of filter coefficients similar to the overall model in the equations of Appendix 2.

Refer to voice communication in GSM. The codec is known as RPE-LTP. The voice is sampled every 20 ms and the actual output signal is a 260 bit block, which is processed as in Section 3 and input to the modulator (Section 5). The block is a representation of a number of different characteristics of human speech as per the previous paragraph. Since the characteristics vary in importance, the bits are not of equal value. For signal processing, the block is divided into two main categories – 182 bits are knows as CLASS 1 and the remaining 78 as CLASS 2. These two sub-blocks are processed separately in accordance with the various operations in Section 3. There is a considerable difference between LPC at 260 bits every 20 ms (i.e., 13 kbits/second) and ADPCM at 32 kbits/second. LPC has major advantages and further research is needed.

Appendix 4: Integrated Services Digital Network (ISDN)

This has no direct connection with GSM, but it is envisaged that the two systems will be able to interface with each other. GSM is cellular radio, whereas ISDN is designed to provide a very comprehensive range of telecommunication services, especially data, via the public telephone network. It does not have a radio facility. Although voice is still the principal form of traffic, data has been growing steadily over the years. The requirement for the integration of voice and data within the same service was essentially market driven.

ISDN is an all digital system from ened to enmd. The voice is digitized using ADPCM and transmitted along with other data on a traffic channel at 64 kbits/second. This type of channel is known as the B Channel to signify bearer. Control signals are transmitted at 16 kbits/second on a different channel, called the D Channel. The standard interface consists of two B Channels, which are totally separae from one another, and one D Channel. Hence, the term 2B+D is often used.

Appendix 5: Cyclic codes

Let: n = block size
$(x^n + 1)$ = modulus
$g\,(x)$ = generator polynomial
$w\,(x)$ = code word represented by a polynomial of degree $(n - 1)$ or less.

In the majority of applications of such codes, $g\,(x)$ and $w\,(x)$ are factors of $(x^n + 1)$. The check bits are chosen such that $g(x)$ divides $w(x)$. In Section 3 the position is as follows:

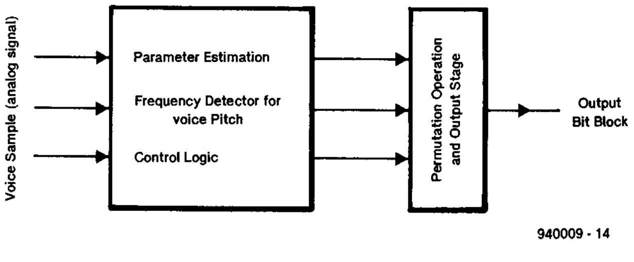
Voice Sample (analog signal)
Parameter Estimation
Frequency Detector for voice Pitch
Control Logic
Permutation Operation and Output Stage
Output Bit Block
940009 - 14

Fig. 3. General arrangement for LPC codec.

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$n = 53$ and $(x^{53} + 1)$ is the modulus

$$g(x) = (x^3 + x + 1).$$

There is a total of eight residue polynomials: 0, 1, x, $(x + 1)$, $(x^2 + 1)$, $(x^2 + x)$, $(x^2 + x + 1)$. The mathematical properties of the encoding operation are:

$$(x^{53} + 1) = A(x)(x^3 + x + 1) + (x^2 + x + 1)$$

$$w(x) = d_0x^{52} + d_1x^{51} + d_2x^{50} + \ldots + d_{49}x^3 + c_0x^2 + c_1x + c_2$$

$$= B(x)(x^3 + x + 1) + (x^2 + x + 1).$$

Thus, $(x^{53} + 1)$ and $w(x)$ have the same residue polynomial modulo $(x^3 + x + 1)$. In Set Theory, they are in the same equivalence class. Any element of such a class is fully representative of that class.

Appendix 6: Convolutional code

From the equations in Section 4:

$$u_{n-2} = (v_{3n} + v_{3n+2}) \bmod 2$$

$$\therefore\ u_n = (v_{3n+6} + v_{3n+8}) \bmod 2.$$

The sequence of calculations at both ends is

Transmitter

$$v_{3n} = u_n + u_{n-1} + u_{n-3} + u_{n-4} \bmod 2$$

$$v_{3n+1} = u_n + u_{n-2} + u_{n-4} \bmod 2$$

$$v_{3n+2} = u_n + u_{n-1} + u_{n-2} + u_{n-3} + u_{n-4} \bmod 2$$

Receiver

$$u_{n-2} = v_{3n} + v_{3n+2} \bmod 2$$

$$u_{n-1} = v_{3n+3} + v_{3n+5} \bmod 2$$

$$u_n = v_{3n+6} + v_{3n+8} \bmod 2$$

If an error occurs in v_{3n+6} or v_{3n+8}, such that the calculated u_n is incorrect, this can be detected by calculating v_{3n}, v_{3n+1} and v_{3n+2} from the deduced u_{n-4}, u_{n-3}, u_{n-2}, u_{n-1}, and u_n. If these do not equal the values received, u_n should be corrected. END

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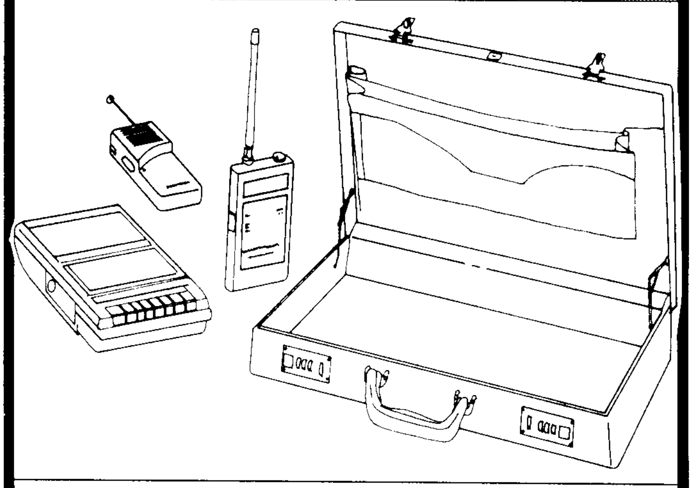

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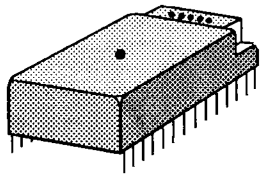

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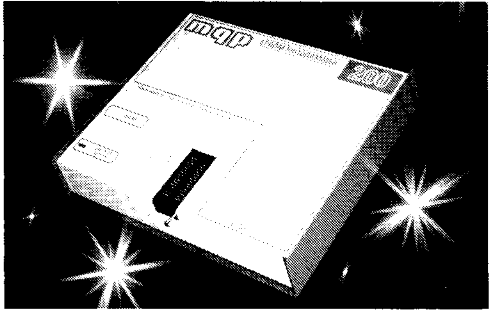

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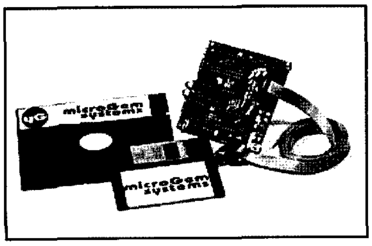

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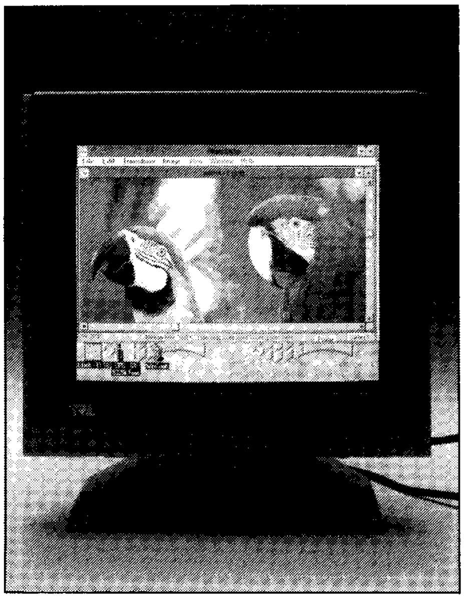
Today, the choice of a monitor for your PC is limited to monochrome VGA or colour VGA. Both types of monitor are driven by a VGA video card which supplies analogue colour signals. This article discusses a low-cost adaptor that gives a significant improvement in grey value rendering when a monochrome display is connected to a VGA card.



Design by T. Scherer

THE decisive factor in the choice between a colour and a monochrome (black and white) monitor is usually cost. If the budget is tight, most beginning computer enthusiasts opt for a monochrome display, which, they are informed by shop assistants, is capable of translating colour drive signals into corresponding shades of grey.

There are two good reasons to choose a monochrome VGA display. Firstly, it is considerably cheaper than a colour type, the price difference being of the order of £100-200. Secondly, colour may not be required, for instance, if your work on the PC is limited to word processing.

Most modern PCs have a built-in 256-colour VGA card. Just in case you think you have missed out on a few developments in the PC scene, anything 'below' VGA, i.e., CGA, EGA, MGA and Hercules, is hopelessly out of date, obsolete, and simply not used any more. Today's standard is the VGA video card, which is almost invariably a colour system, and usually capable of emulating all of the older standards. Although a monochrome mode is available on most VGA cards, this is rarely if ever used because it is a very poorly supported feature. So, colour it is, but how will it look on a monochrome monitor?

Unfortunately, if a monochrome monitor is connected to a VGA card, the resulting picture quality leaves much to be desired, mainly because the monitor translates the intensity value of a particular colour into a corresponding grey level. Alas, this conversion is far from perfect, and some colours are virtually lost. Even a cursory look at the problem reveals that it is caused by imperfections in the design of the link between the VGA card and the monochrome display. The fault is fairly obvious: the monitor looks at only one colour signal supplied by the VGA card, while the other colour signals are simply not used. Fortunately, this shortcoming is easily overcome with a circuit that costs next to nothing, yet gives a significant improvement in the quality of the picture as it appears on your monochrome VGA screen.

The eyes have it

The picture quality on a monochrome VGA screen driven by a VGA card can be optimized by ensuring that every colour is properly converted into a corresponding grey level. As already mentioned, most inexpensive monochrome VGA monitors use only one colour signal, usually red or green, to write the picture. The result of this far too simple conversion is that some picture details are completely lost, while others appear as black blocks.

A proper conversion of the three primary colour signals, R, G and B, into a monochrome picture can be achieved at practically no cost. All you require are a couple of resistors that combine the three colours into a composite signal. However, the signals can not be coupled just like that, and the values of the resistors need to be given some consideration.

The human eye has different sensitivities for the three basic colours, red (R), green (G) and blue (B). Extensive research has shown that the brightness, or luminance (Y), of a picture must be composed as follows:

$$Y = 0.3R + 0.59G + 0.11B.$$

The equation shows clearly that up to 40% of the picture contents are lost if, for instance, only the green component is used to generate the Y signal. Obviously, a colour picture can only be faithfully displayed on a monochrome monitor if the colour components are added ('summed') at the ratios given by the above equation.

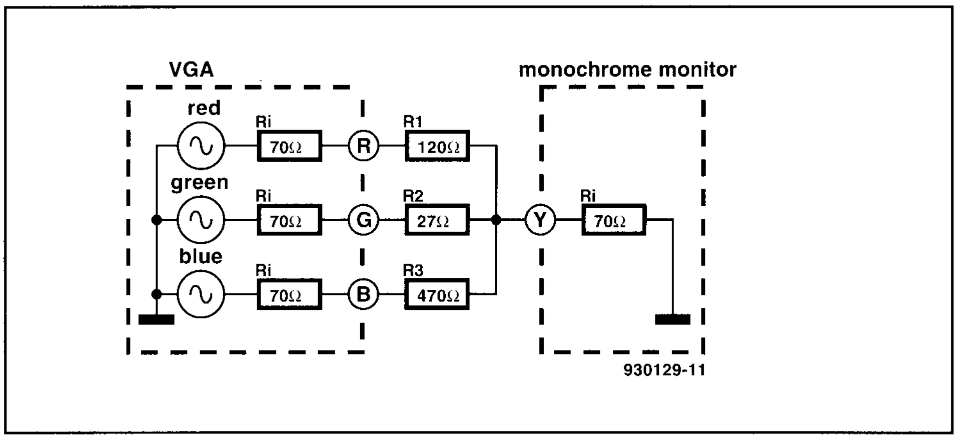


Fig. 1. Luminance summing network in which input and output impedance requirements have been disregarded.

The circuit

Turning the above theory into practice, i.e., implementing the summing network, is not as easy as one would expect. A complicating factor is the need of maintaining an impedance of about 70 Ω at the monitor input and each of the outputs on the VGA card. **Figure 1** shows a network that complies with the above luminance equation, but pays little attention to the characteristic impedance requirement. This creates a mismatch between the monitor and the VGA card. Inevitably, some resistors have to be added to make sure that both the card and the monitor 'see' an impedance of 70 Ω. **Figure 2** shows an extended schematic in which resistors R_{m1}, R_{m2} and R_{m3} serve to correct the terminating impedance of the VGA card, while resistor R_{ms} does the same for the source impedance of the monitor input.

The number crunching needed to come up with the correct resistor values was left to a computer. The result is shown in **Fig. 3**. It will be noted that R_{ms} and R_{m2} shown in Fig. 2 are missing. The reason is simple: they have such a high value (>10 kΩ) as to have no effect on the effective impedances. Fortunately, it was possible to round off the resistance values such that ordinary resistors from the E12 series could be used (resistor R_3 consists of two 120-Ω resistors connected in series). Although 1% resistors may be used, the conversion accuracy of the network is more than sufficient if you use 5% types.

With some dexterity, the six resistors may be built into the monitor's sub-D15 plug, provided this is not a moulded, riveted or otherwise completely sealed type. To cut down cost, many monitor manufacturers omit non-used pins on the D15 connector. Unfortunately, that means that you have to purchase a new connector.

Before you start soldering, cover the inside of the connector with insulating tape. This prevents short-circuits with the metal layer which is often damped onto the plastic connector hoods. The photograph in **Fig. 4** shows the author's prototype of the adaptor.

After installing the VGA adaptor network, the monitor should show a picture with perfect grey levels, and no picture elements missing. If not, check the settings of the VGA card, and those of the brightness and contrast controls on the monitor. As regards the VGA card, be sure to have this running in 256-colour mode, not, of course, in any of the (primitive) monochrome modes. ■

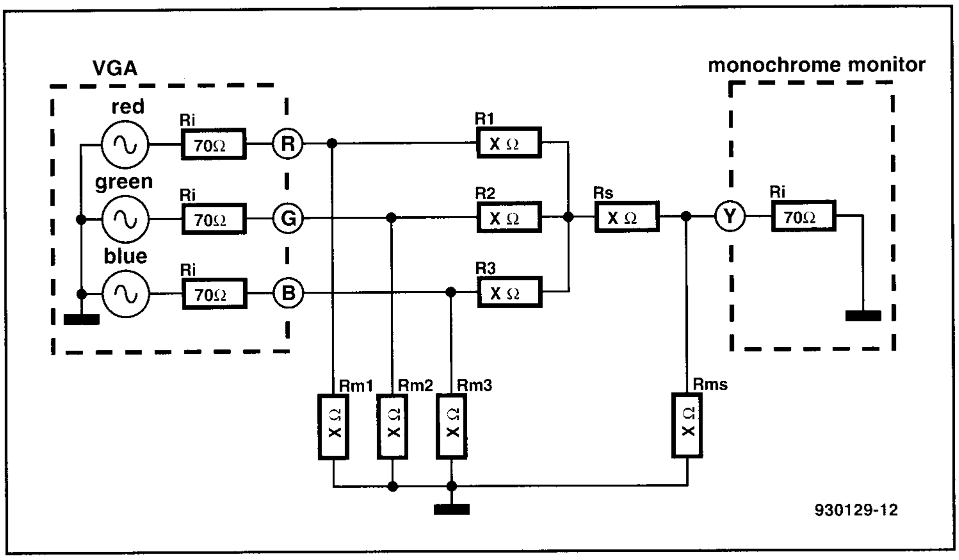


Fig. 2. The same as Fig. 1, but taking into account a certain input and output impedance.

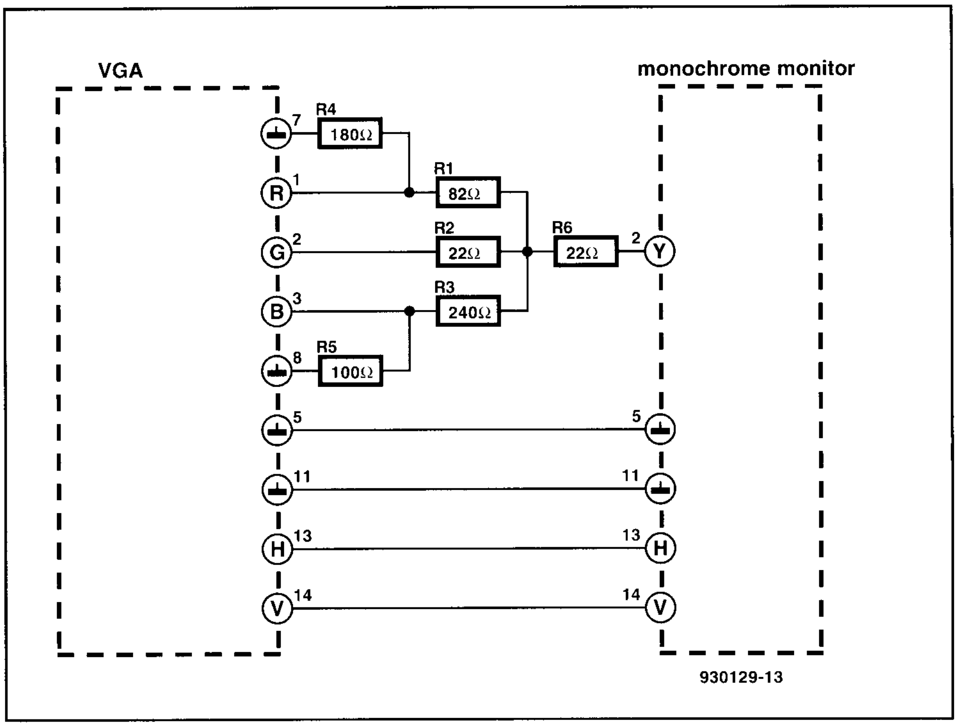


Fig. 3. From theory to practice. Circuit diagram of the monochrome VGA adaptor.

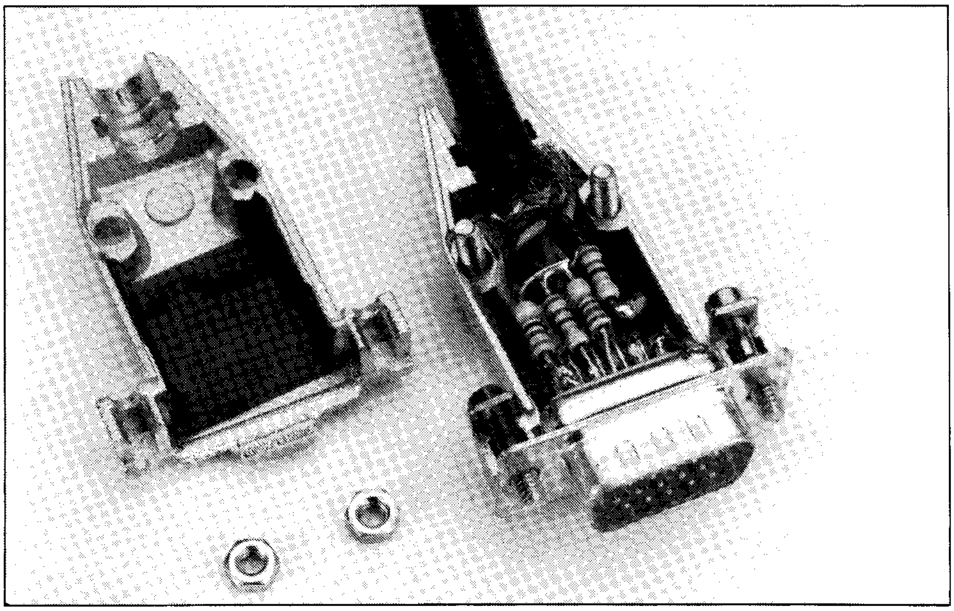


Fig. 4. Prototype of the adaptor network fitted into a 15-way sub-D connector.

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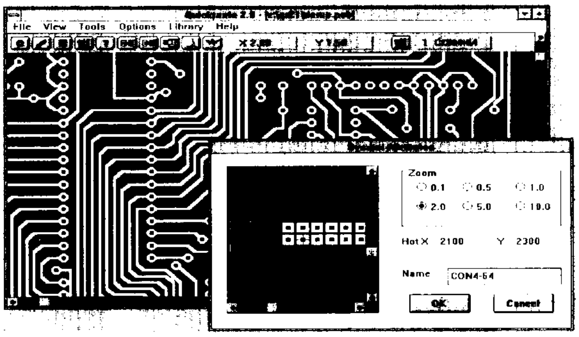

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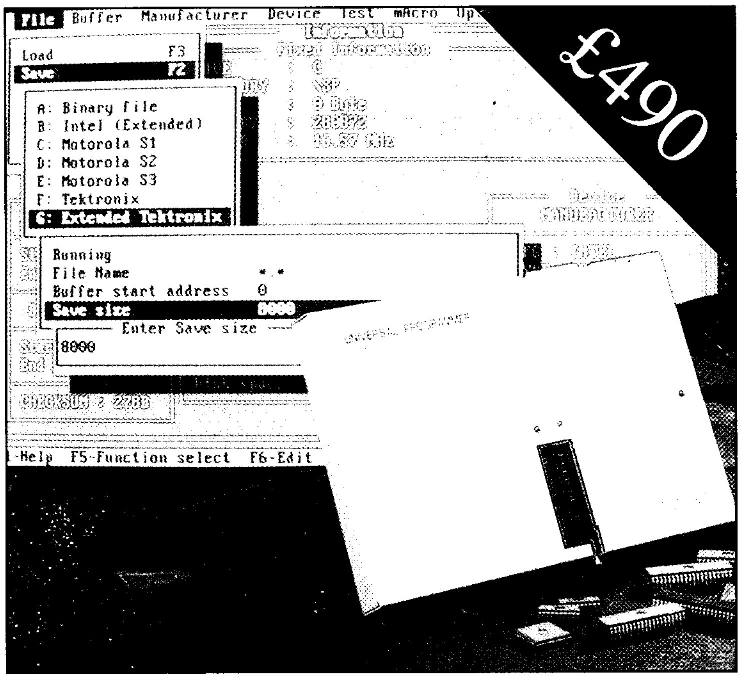

```
Load                F3
Save                F2

A: Binary file
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D: Motorola S2
E: Motorola S3
F: Tektronix
G: Extended Tektronix

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File Name                 *.*
Buffer start address      0
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8000

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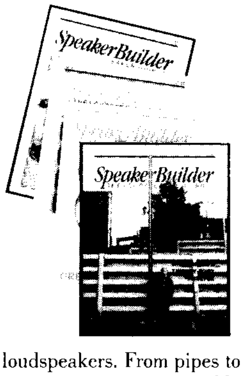

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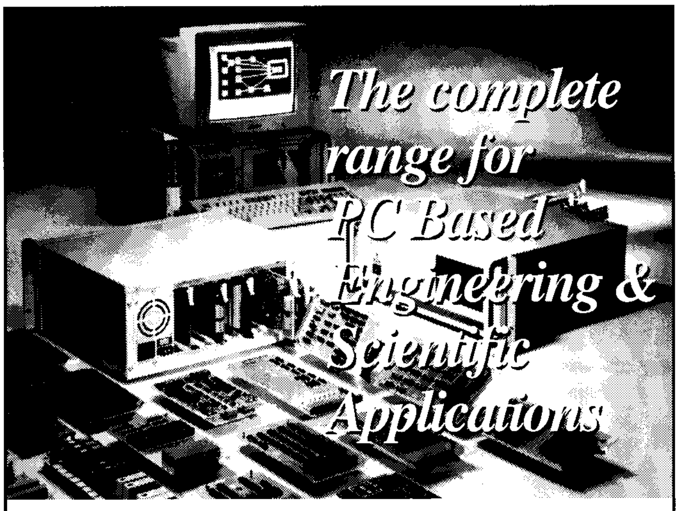
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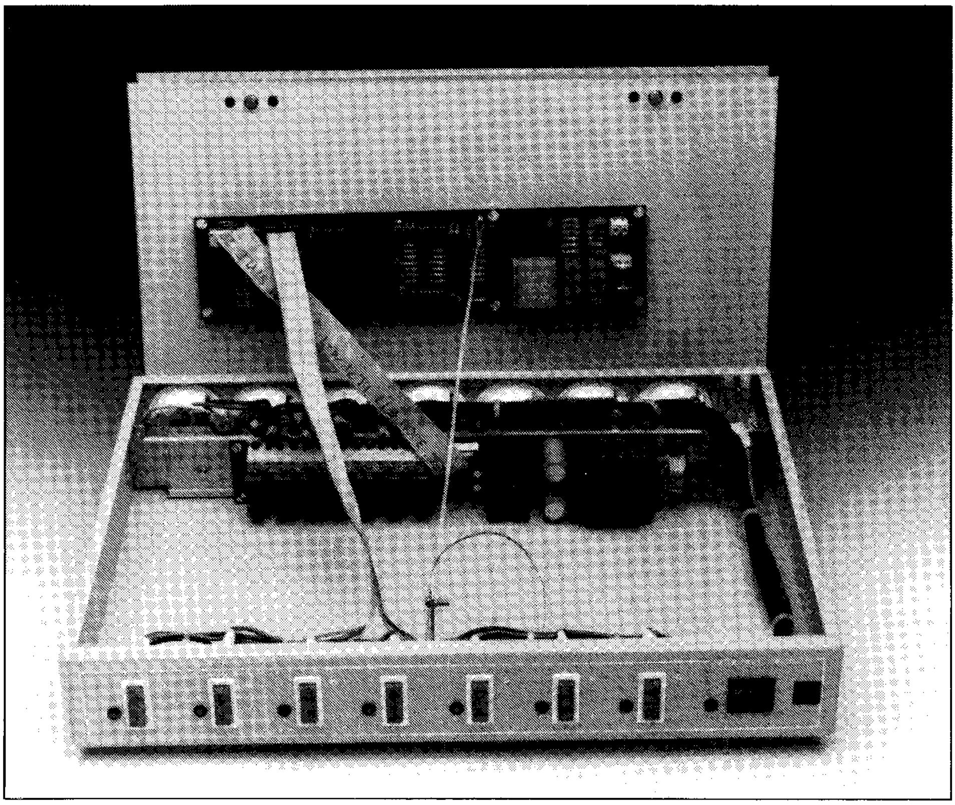

The switching unit described here is capable of controlling up to seven mains-powered loads with the aid of commands received via telephone. Any tone-dialling (DTMF) telephone set or hand-held tone dialler may be used to send commands to the switching unit, and remotely control a wide range of mains appliances in and around the home. With personal access code and system feedback!

Design by F. Zapf

THE circuit is connected to the telephone network* just like any normal telephone set. On being called, the circuit waits a predetermined number of ring signals, and then answers the call (electrically, it 'lifts the receiver'). Next, it waits for a pre-programmed system access code, which the caller must transmit with the DTMF keypad on his telephone.

The unit is capable of switching up to seven loads on and off. By virtue of relays, high voltages and currents may be switched, so that loads may include mains-powered ones. Reception of the correct system code is acknowledged with a short tone, which the caller can hear. Next, load number '1', for instance, a coffee machine, may be switched on by pressing the '1' key two times. The same load is switched off by dialling 1 and then 0. The status of load '1' (on or off) may be called up by pressing 1 and then 2 on the DTMF keypad. The switching unit responds to this by two short tones to signal that the load is on, or a single long tone to signal that the load is off. The control of the other six loads is identical to that of load '1', i.e., the channel (load) number is dialled first, then 0 or 1 for switching off or on, or 2 to request the channel status. An exception is formed by number 8: dialling this number allows you to switch all channels on or off simultaneously. On/off status requesting does not work in this mode.

The circuit

The heart of the circuit diagram, given in **Fig. 1**, is formed by an 8031 microcontroller. The computer control section sits between a telephone interface circuit and a power switching interface. An integrated DTMF decoder Type MV8870 (**Fig. 2**) decodes the tone dialling codes received via the telephone line.

The telephone line interface consists of two parts: one to detect the ring signals that enables the unit to answer the call at the right moment, and another to receive and transmit tones via the telephone line.

The ringing signal detector is relatively simple. A bridge rectifier, D_3-D_6, connected to the telephone lines ('a' and 'b') turns the ringing signal (an alternating voltage) into a pulsating direct voltage, which is smoothed by C_3, and limited to 15 V with the aid of zener diode D_7. The direct voltage across D_7 supplies the LED in optocoupler IC_7, with resistor R_9 acting as a current limiter. During the ringing signal, the collector of the phototransistor in the optocoupler (pin 8) is at ground potential. The microcontroller, IC_1, interrogates the state of the optocoupler output signal via port line P1.7. To suppress error pulses, the low level at the optocoupler output is also used to trigger monostable multivibrator (MMV) IC_6. The MMV's monotime is started by the ringing signal, and supplies a logic high level to microcontroller pin INT0/P3.2 for about 10 seconds. This is the period available for transmitting codes to the switching unit. As long as the circuit has not 'lifted the receiver', i.e., as long as relay Re_1 is not energized, the MMV is triggered again via the RET connection.

The coupling with R_7-C_2 ensures that the ringing signal detector responds to alternating voltage only. Any direct voltage levels that may exist between terminals 'a' and 'b' are ignored. An LED, D_{10}, provides a visual indicator for the call and DTMF signals.

When the microcontroller has counted the programmed number of ringing pulses, it responds by pulling output P1.6 logic high, which causes relay Re_1 to be energized via R_6 and T_1. This means that the switching unit 'lifts the receiver', i.e., answers the

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* The term 'telephone network' in this article refers to a closed system installed in the home or office. The switching unit described here is **not** BT type-approved for connection to the Public Telephone Network (PTN).

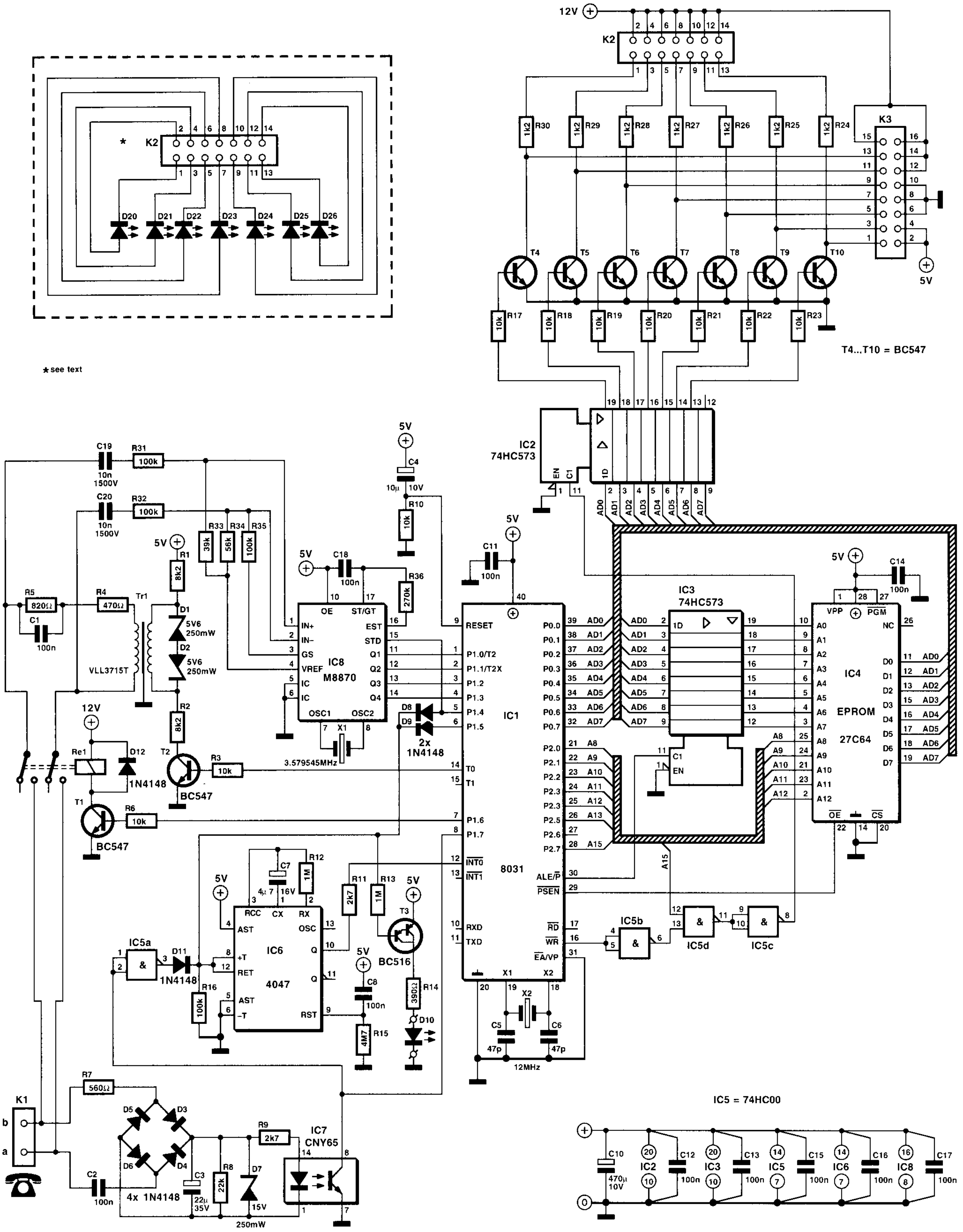

Fig. 1. Circuit diagram of the telephone-controlled DTMF switching unit — a typical microcontroller application circuit based on a 8031.

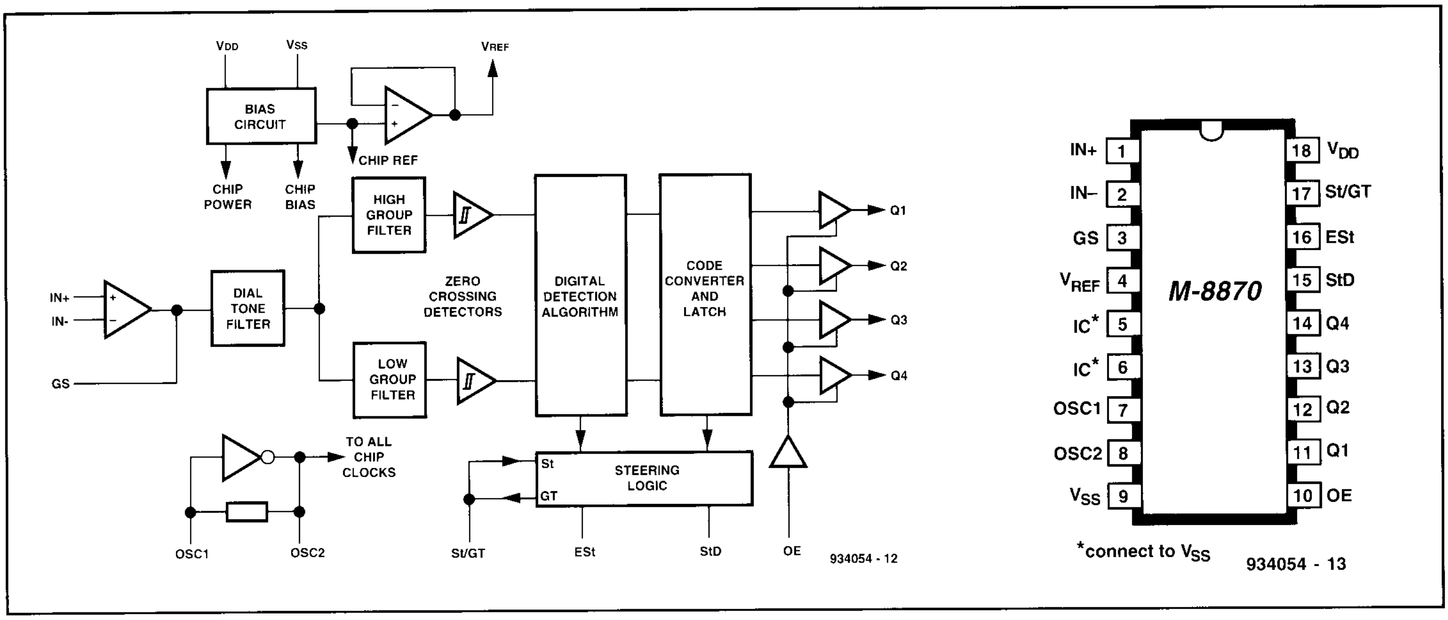

Fig. 2. Internal structure and pinning of the M-8870 DTMF decoder from Teltone (second source: Plessey Semiconductors).

call. Consequently, the series network R4-R5 and the primary winding of telephone line transformer Tr1 is connected to the 'a' and 'b' lines via the relay contacts. The current flowing through this network is sufficiently large to maintain the connection. One end of the transformer secondary winding is connected to the positive supply voltage via R1, while the other end is connected to ground via R2 and T2. This means that rectangular volt-

COMPONENTS LIST

Resistors:

2	8kΩ2	R1;R2
10	10kΩ	R3;R6;R10; R17-R23
1	470Ω	R4
1	820Ω	R5
1	560Ω	R7
1	22kΩ	R8
2	2kΩ7	R9;R11
2	1MΩ	R12;R13
1	390Ω	R14
1	4MΩ7	R15
4	100kΩ	R16;R31;R32; R35
7	1kΩ2	R24-R30
1	39kΩ	R33
1	56kΩ	R34
1	270kΩ	R36

Capacitors:

4	100nF MKT	C1;C2;C8;C18
11	100nF ceramic	C11-C17;C22; C23;C26;C27
1	22µF/35V radial	C3
1	10µF/10V radial	C4
2	47pF	C5;C6
1	4µF7/16V radial	C7
2	100µF/25V radial	C9;C24
1	470µF/10V	C10
2	10nF/1500V MKT	C19;C20
2	1000µF/35V radial	C21;C25

Semiconductors:

1	B40C1500/1000	B1
2	zener 5V6/400mW	D1;D2
16	1N4148	D3-D6;D8;D9; D11-D19
1	zener 15V/400 mW	D7
1	LED red 3mm (w. mounting clip)	D10
6	LED green 3mm (w. mounting clip)	D20-D26
9	BC547	T1;T2;T4-T10
1	BC516	T3
1	8031 or 80C31	IC1
2	74HC573	IC2;IC3
1	27C64 (order code 6271; see page 70)	IC4
1	74HC00	IC5
1	4047	IC6
1	CNY65	IC7
1	M8870 (Teltone)[1;5] or MV8870 (Plessey Semiconductors)[2]	IC8
1	7812	IC9
1	7805	IC10

Miscellaneous:

1	Fuse 100mA slow	F1
1	PCB terminal block, pitch 5mm	K1
1	14-way box header and IDC socket	K2
2	16-way boxheader and IDC socket	K3;K12
8	PCB terminal block, pitch 7.5mm	K4-K11
1	V23037-A0002-A101 (Siemens)[3,5] (DPDT; 12V/250V/5A)	Re1
7	V23127-B0002-A101 (Siemens)[3,5] (SPDT; 12V/250V/5A)	Re2-Re8
1	VLL3715T[5]	Tr1
1	Mains transformer 15V/8VA (e.g., Monacor/Monarch[4] VR8115)	Tr2
1	Crystal 3.579545MHz	X1
1	Crystal 12MHz	X2
1	Heat-sink SK129/25	
1	Type 'Power Manager' case; Conrad[6] order code 999008-11	
1	Printed circuit board and EPROM 6271, set order code 934054 (see page 70)	

[1] Chesilvale Ltd., 10 Woodland Road, Clifton, Bristol BS8 1 UQ. Telephone: (0272) 736166, fax (0272) 736516.

[2] 2001 Electronic Components (0438) 742001; Celdis Ltd. (0734) 585171; ESD Distribution (0279) 441144; Farnell Electronic Components (0532) 636311; Gothic Crellon Ltd. (0734); Semiconductor Specialists (UK) (0895) 445522; Unitel Ltd. (0438) 312393.

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[5] C-I Electronics, P.O. Box 22089, 6360 AB Nuth, Holland. Fax: (+31) 45 241877.

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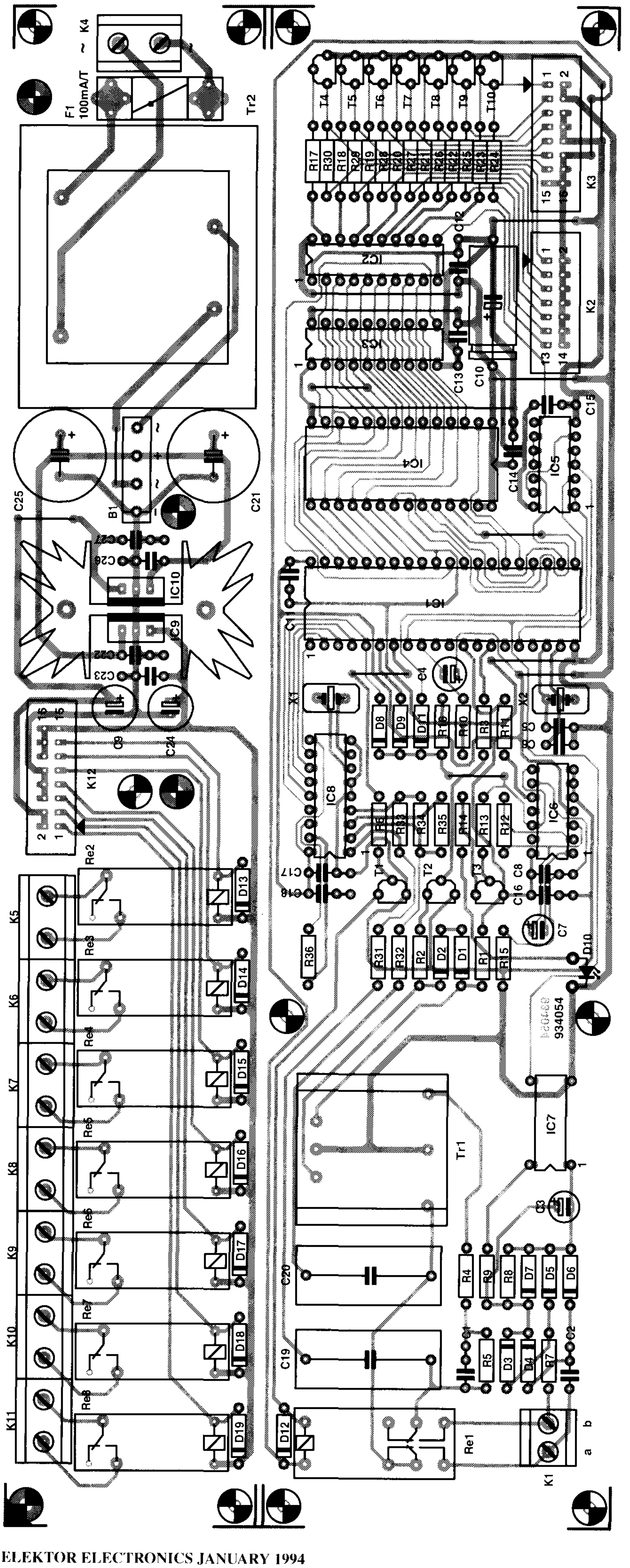

ages generated by the controller on line T0/P3.4 are coupled directly on to the telephone network lines. Two zener diodes, D1 and D2, limit the voltage across the secondary winding to safe levels.

The received DTMF signals are capacitively coupled to the decoder, IC8. The external components that enable the M8870 DTMF decoder to operate reliably are limited to four resistors, a capacitor and a quartz crystal. The four decoder outputs, Q1-Q4, supply a bit pattern that corresponds to the received DTMF number, sign or letter. The structure of the bit pattern is given in **Table 1**. The 4-bit DTMF code is applied to the microcontroller via port lines P1.0 to P1.3.

The microcontroller has its external address (EA) line tied to ground, and fetches its instructions from an external 8-KByte EPROM Type 27C64. The address and data signals are demultiplexed at port P0 by an 8-bit latch Type 74HC573. A RAM IC is not found in this application, since it is not required to store large amounts of data. The only two user programmable parameters, the number of ringing signals and the 'access code', are conveniently stored in the controller's internal RAM. A second 8-bit latch with three-state outputs, IC2, allows the controller to output 8-bit words. Seven of the eight latch output bits Q1-Q8 are used to control relays Re2 to Re8 and LEDs D20 to D26 via driver transistors T4-T10. Both the relays and the LEDs are 'commoned' to the 12-V positive supply rail. This enables 'true' logic to be used, i.e., a logic one at latch output Q1-Q7 switches the associated relay on. Flyback diodes D13-D19 protect the switching transistors against back-e.m.f. surges produced by the relay coils when these are switched off.

The power supply of the telephone-controlled switch is conventional, and based on fixed voltage regulators. The 12-V and 5-V supply voltages used for the relay sections and the digital sections respectively are derived from a single mains transformer with a secondary voltage of 15 V.

Construction

The artwork of the single-sided printed circuit board designed for the telephone controlled switch is shown in **Figs. 3a and 3b**. The board consists of two parts. One accommodates the mains transformer, the power supply and the relays, the other, the tele-

Fig. 3a. Component mounting plan of the printed circuit board designed for the telephone-controlled switch.

phone line interface and the microcontroller circuit. Before you start fitting parts, separate the two boards by cutting.

Populating the boards is straightforward since the component densities are fairly low. It is good practice to start with the low-profile parts, followed by the taller and larger ones.

On the component overlay, small triangles indicate the position of pins '1' of boxheaders or pin headers K2, K3 and K12. Boxheaders are preferred here because of their greater stability and orientation notches, which make it impossible to insert the flatcable connector the wrong way around.

The channel activity LEDs, D20 to D26, are not fitted on to the board. It is suggested to mount these LEDs on to the enclosure front panel, near the device on/off switches, and connect them to the board via a length of flatcable and press-on (IDC) connectors.

The eight connectors marked with asterisks (*) in the wiring diagram in **Fig. 4** are the seven mains sockets to which the loads are connected, and the mains input socket.

Mechanical construction

The presence of the mains voltage in the circuit rules that the enclosure of the telephone-controlled switch be electrically safe in all respects. To meet this requirement, and to keep mechanical work to a minimum, the prototype of the telephone-controlled switch was built into a 'Power Manager' case supplied by Conrad Electronics. This case is basically an on/off switching unit for seven mains powered devices. The case only contains wiring, a mains inlet, seven switches plus neon lamps, and seven mains sockets to which appliances are connected. The switches on the front panel allow each appliance to be individually switched on and off. The case contains no electronic parts, only electromechanical parts and wiring.

The holes in the relay board are located such that the board is easily secured on to the mounting screws for the mains socket strip in the Power Manager case. The board is secured with the aid of M4 (4-mm) PCB standoffs and screws. The other board is fitted on to the enclosure bottom plate with the aid of PCB spacers, nuts and screws. Finding a suitable location for the board is not a problem because there is plenty of space.

The actual construction of the

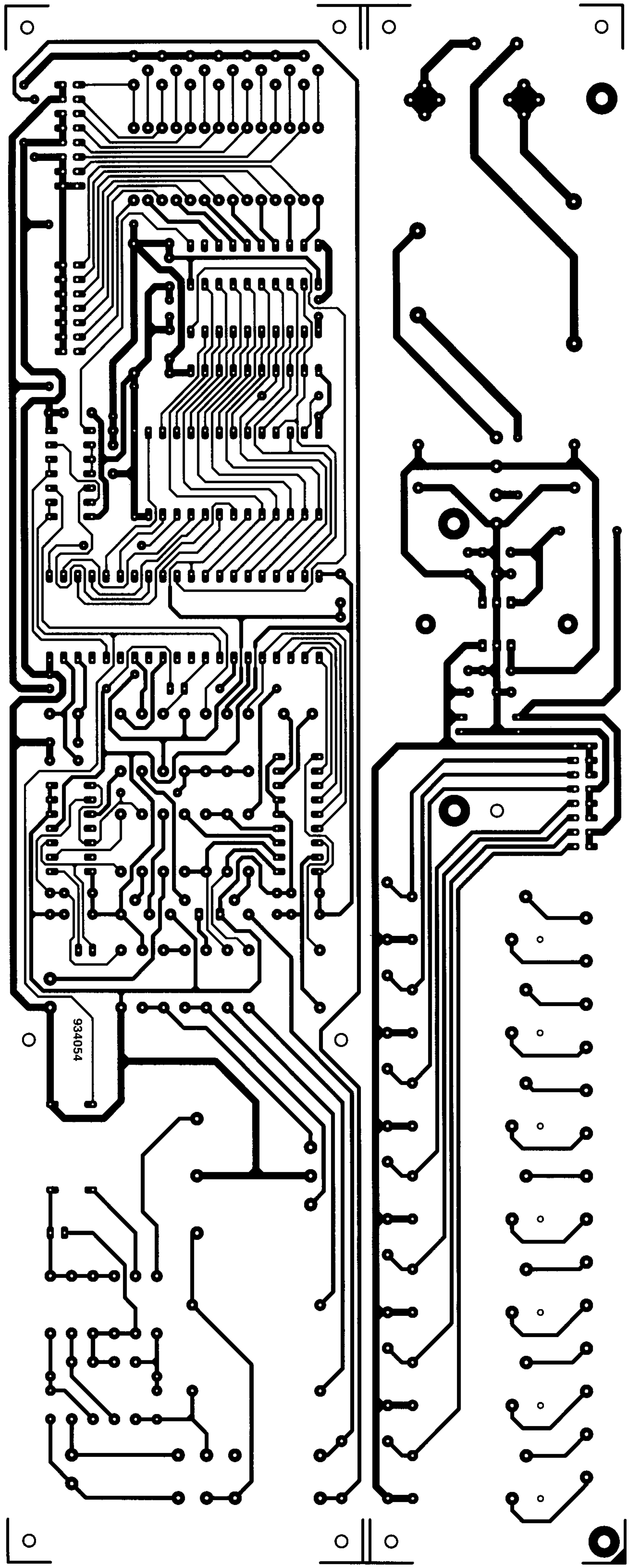

Fig. 3b. Track layout (direct reading) of the PCB designed for the telephone-controlled switch.

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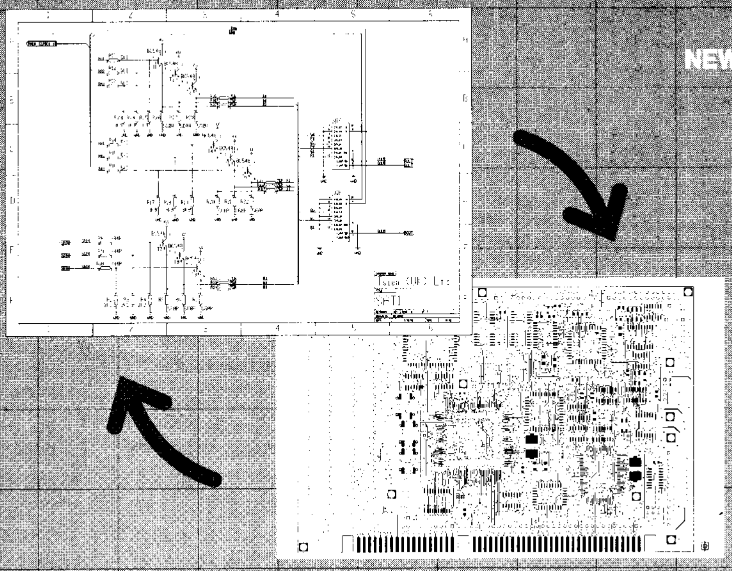

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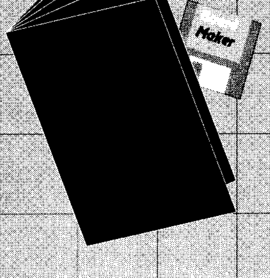

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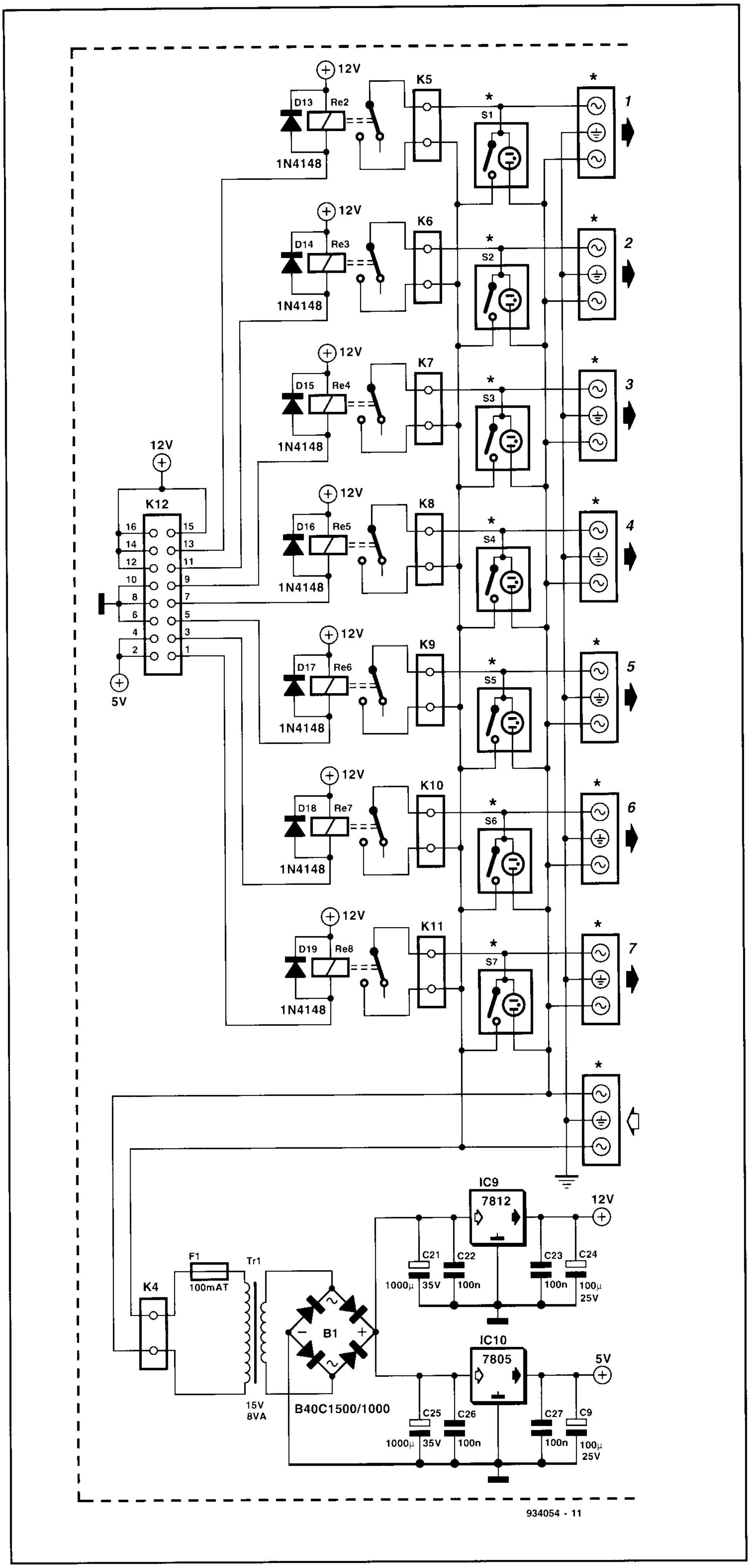

Fig. 4. Circuit diagram of the power supply and mains/switching sections.

Power Manager case is a little unusual. The switches and the mains sockets are fitted on to the angled front and rear part, respectively, of the cover plate. Since all wires run underneath the cover plate, travelling the distance between the switches and the sockets, the free space inside the case is almost fully crossed by wires. If you want to construct your switching unit like our prototype, it is, unfortunately, necessary to install completely new wiring, and bundle wires in neat trunks.

Operation

Apart from the central on/off switch and the channel on/off switches on the front panel, the telephone-controlled switch has no local controls. All commands reach the unit via the telephone line in the form of DTMF codes generated on a telephone set with a tone dialling keypad, or a pocket tone dialler. Commands are, obviously, only accepted if the unit has answered the call. Wrong commands or pauses longer than 10 seconds cause the unit to transmit a long signal and then ring off.

As already mentioned, the commands consist of two numbers pressed on the telephone keypad. The first number is the channel number, 1 through 7, and the second number is either 0 (channel off), 1 (channel on), or 2 to request the on/off status of the channel.

Pressing 8 followed by 0 or 1 switches all channels off or on respectively.

The **system access code** is a kind of personal identification number (PIN) that prevents non-authorized use of the switching unit. To program or reprogram the system access code, wait for the unit to answer your call, and then dial ***1**. The unit responds with two short signals. You now have several options. Pressing # disables the access protection, and clears the existing access code. This is confirmed by the unit producing a long and a short signal, and then ringing off.

To overwrite or program an access code for the first time, the desired code is entered following the *1. The code can have up to eight numbers, and the unit confirms reception of each of these by a short signal. The sequence is terminated by pressing the # key, which, consequently, can not be part of the system access code. On receipt of the # tone, the unit transmits a long and a short signal. Pressing # is not required if the access code consists of exactly eight numbers. The new access code is retained until it is overwritten, or the unit is switched off and on again. When this happens, the access

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code is automatically changed into 123456.

The **number of ringing pulses** is programmed by calling up the unit, and then pressing ***2**. The unit will respond by transmitting two short signals. Next, enter the desired number of ringing pulses before the unit will answer a call. First enter the tens (0, 1 or 2), then the units (1 through 9). Each acceptable entry is confirmed by the unit transmitting a short signal. Reception of a wrong number causes the unit to transmit a long signal and then break the telephone connection. If the number of ringing pulses is accepted, the unit responds with an interrupted signal, whereupon it rings off. The programmed number is retained until it is overwritten, or reset to the default value of 6 when the unit is switched off and on again.

The third special function is the **DTMF transmitter test**, which is invoked by calling the unit, and pressing ***3**. In this mode, the unit responds to the number pressed on the telephone by generating a corresponding number of short signals, for instance, four if your press the '4' on your telephone. Pressing the *, # or letter code (A-D) keys should produce 11, 12 or 13 through 16 short signals. A pause longer than 10 seconds prompts the switching unit to ring off. ■

Key	OE	Q4	Q3	Q2	Q1
1	1	0	0	0	1
2	1	0	0	1	0
3	1	0	0	1	1
4	1	0	1	0	0
5	1	0	1	0	1
6	1	0	1	1	0
7	1	0	1	1	1
8	1	1	0	0	0
9	1	1	0	0	1
0	1	1	0	1	0
*	1	1	0	1	1
#	1	1	1	0	0
A	1	1	1	0	1
B	1	1	1	1	0
C	1	1	1	1	1
D	1	0	0	0	0
other	0	*	*	*	*

* = output at high-impedance

Table 1. M8870 DTMF decoder output codes as a function of received tone pair. The OE (output enable) input allows all outputs to be switched to high-impedance.

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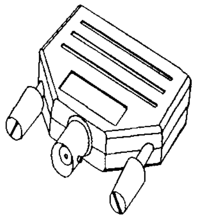

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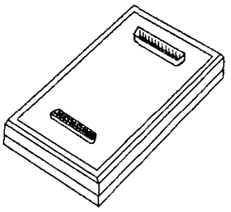

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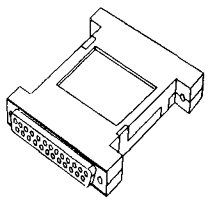

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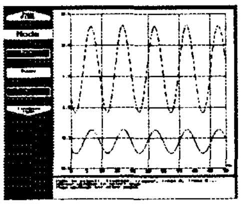

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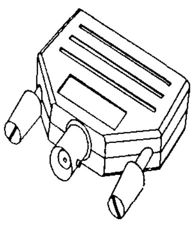

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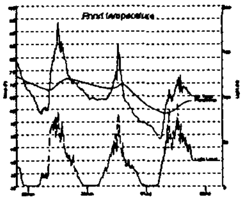

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DX TELEVISION

A two-monthly column by Keith Hamer and Garry Smith

SUSTAINED openings throughout August gave way to a dramatic drop in sporadic-E activity within the first few days of September. On the whole, the season has been a satisfying one for most long-distance TV enthusiasts, despite it being a comparatively short one.

Reception from the Middle East has been less favourable for DX-ers in the United Kingdom this season, whereas in Europe Iranian transmissions have been regularly identified on channels E2, E3 and E4. To make up for this, enthusiasts in the United Kingdom have witnessed at least three transatlantic openings this season, albeit short ones. Although late August is not traditionally an 'exotic' period, the 22nd brought in 525-line signals on channels A2 and A3 for ten minutes for Simon Hamer in New Radnor (Powys). During the same opening, Band III sporadic-E signals were evident from Iceland on channels E6 and E7, and later from Denmark on channel E5. This is the only reported incidence of Band III sporadic-E reception so far this season. Simon had virtually an identical pattern of reception in early June 1988, and two days later signals from Algeria, Libya and Tunisia were seen in Band III. Unfortunately, these signals were not around on this particular occasion!

August 21st was also an action-packed day, with continuous reception from early morning until late at night. Signals were first noted from Scandinavia, then Central Europe, with favourable reception from stations to the south-east and south during the early evening.

September saw a sudden decline in activity with signals mainly from the south on the 4th and 5th. The last opening of any significance occurred on the 10th with signals from Scandinavia and Spain in evidence throughout the day.

Reception reports

Tim Webbs (New Romney) watched excellent-quality tropospheric signals from Belgium, France and the Netherlands on September 8th, using an Antiference XG14 wideband array, without a mast-head amplifier. Of particular importance was his reception of 'Zuid-Holland TV', a new regional station on channel E49 with an ERP of around 10 kW. At the time of his reception (1845 UTC), colour bars were being transmitted.

Iain Menzies (Aberdeen) has recently returned from the French Alps, with news of DX-TV possibilities there. During his visit, Iain logged NRK, TVE, RTP and some stations from the former Yugoslavia in Band I. Tropospheric reception on channel E4 from La Dôle in Switzerland, and a French station just above E4 (channel L4) were evident. RAI Uno on channels IA and IB also appeared by tropospheric enhancement on some evenings.

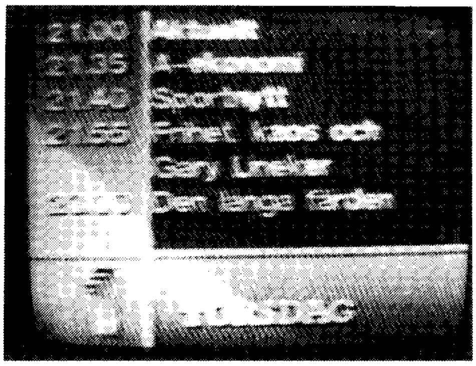
Chris Howles (Erdington) reports a mystery 'JRT BGRD-1' (Serbia) PM5544 test card seen on channel R2 during the second half of August. The test pattern was floating with other known channel R2 signals, thus confirming the frequency. One possible explanation is that an Eastern European country was relaying Serbian TV from Eutelsat II-F4. The Serbian TV logo 'PTC B1' has also been seen on channel R1 by other enthusiasts.

Marc Vissers (Belgium) has received most of the 'usuals' this summer, such as TVE-1, RTP-1, RAI UNO, OK-1 (Russia) and HTV-1 (Croatia). In addition, some rarer signals were noted including MRT-1 (Macedonia), and surprisingly TV Shqiptar (Albania) on channel C. This latter transmitter is no longer listed in the WRTH 1993, but the station was identified by the PM5534 test card, indicating that it is still on-air.

Stephen Michie (Bristol) comments that August was quite reasonable with CIS programmes being seen from Latvian transmitters. Stephen queries Latvia's TV transmitters listed in publications such as the WRTH, and wonders whether these are locally produced services or relays of Ostankino TV (Russia). The identifications used on the G-204 test pattern are also causing concern for may DX-ers. The different idents seem meaningless, and do not indicate the country of origin.

At 1237 UTC on August 15th, Stephen noticed an announcer on channel E4 with the initials 'MRT' in the top right-hand corner of the picture. This signal is thought to have originated from the Pelister transmitter in the south of Macedonia.

Bernd Trutenau (Lithuania) has corrected a news item concerning Lithuania. The channel R11 transmitter is no longer atop the parliament building in Vilnius (it was originally installed there for security purposes during the period of occupation of the facilities of Lithuanian Radio and TV in 1991). Channel R11 programmes are now broadcast from the main TV/FM tower in Vilnius from where the other TV programmes are also aired.



Swedish programme schedule received by Bob Brooks via sporadic-E on channel E2.

Log for August

Sporadic-E reception occurred on most days throughout the month, but only the more prolonged openings are shown below.

12.08.93: Sporadic-E signals between 0605 and 1447 UTC; Sweden E3; Norway E3 and E4; Spain E3; Denmark E3; many unidentified signals on channels R1 and R2.

14.08.93: Reception from 0705 until 1705 UTC: Spain E3 and E4; Italy IA and IB; Czech Republic R2; Hungary R2; Poland R1; Switzerland E2.

21.08.93: An excellent all-day opening between 0844 and 2250 UTC with signals from Sweden E2 and E3; Norway E3; Poland R1, R2 and R3; Denmark E3; Hungary R2; Italy IA and IB; Spain E2, E3 and E4; Portugal E4; Czech Republic R1; Corsica on channel L3.

15.08.93: Signals between 0719 and 0815 UTC: Czech Republic R1; Austria E2a; Italy IA and IB; Norway E2 and E3; Macedonia E4; Germany E2.

22.08.93: Sporadic-E reception between 0851 and 1916 UTC included: Norway E2, E3 and E4; Sweden E2, E3 and E4; Denmark E3, E4 and E5; Poland R1, R2 and R3; Czech Republic R2; Slovakia R2; Spain E2; CIS R1, R2, R3 and R4; Albania IC; USA/Canada A2 and A3; Iceland E3, E4 and E6.

23.08.93: Reception from 0715 until 1330 UTC included: Iceland E4; Portugal E2 and E3; Spain E2, E3 and E4; Italy IA; Hungary R1.

25.08.93: Sporadic-E noted between 0740 and 2105 UTC included: Sweden E2, E3 and E4; CIS R1, R2, R3 and R4; Italy IA and IB; Rumania R3; Poland R1; Finland E4.

26.08.93: Reception between 0845 and 2030 UTC: Norway E2 and E3; Sweden E2 and E3; Portugal E3; Spain E2 and E3; Czech Republic R1; Slovakia R2; Slovenia E3; Germany E2.

30.08.93: Countries identified from 0619 until 1700 UTC included: Italy IA and IB; Corsica L2; Spain E2 and E3; Czech Republic R1; CIS R2; Sweden E2, E3 and E4; Norway E2 and E3; Finland E3; Iceland E3.

Log for September

04.09.93: Sporadic-E reception mostly around midday: Norway E4; France L2 and L3; Spain E2, E3 and E4.
10.09.93: Norway E3; Sweden E2; Spain E2 and E3 (including various regional news programmes around midday).

The DX-TV logs were kindly supplied by Andrew Jackson, Stephen Michie, Simon Hamer, Bob Brooks, Garry Smith and Barry Bowman.

German DAB plans shelved

Plans for the introduction of DAB (Digital Audio Broadcasting) in 1995 have been shelved by ARD due to a shortage of funds. It seems that 1997 will be the earliest possible starting date, depending on whether the EC or the German government will help to finance the project. It will cost at least DM 30 million just to vacate channel E12, which is the part of Band III where DAB transmissions would be.

Service information

Belgium: BRTN is to reduce its airtime as part of a drastic cost-cutting exercise. Needless to say, plans for the introduction of morning television and the extension of afternoon transmissions have been shelved. This is mainly as a result of fierce competition from its commercial rival, VTM, with the resultant loss of advertising revenue. BRTN intends to remain committed to information, education and general entertainment programmes rather than move downmarket, presumably resisting American imports and 'satellite-style' TV. However, BRTN could face further problems when new rules allow Dutch services to be distributed by cable.

The Belgian government is to allow an increase in power (400 W maximum) for 50 MHz amateur operation, with no restrictions on the type of transmitting aerial used.
France: Two new channels (one educational, the other news) may soon be launched by TF1. The educational channel will broadcast during the day via the former La Cinq transmitters, which at present broadcast ARTE from late afternoon onwards.
Netherlands: Programmes are being shown as early as 0700 local time via the NED-1 network.

Identification caption received by Bob Brooks from the Eesti TV (Estonia) transmitter at Tallinn on channel E2.

Omroep Fryslan, a local TV service in the province of Friesland, is planning to be on the air from January 1994, but initially the service will only be available via cable. The proposed channels for the service (from the Franeker transmitter) are E22, E25 and E28 with a maximum ERP of 300 kW.

'Zuid-Holland TV' ('ZH-TV') is now on test on channel E49 with an ERP of approximately 10 kW. The proposed starting date was September 1st, 1993, but by late September test transmissions, consisting of colour bars (with the identification 'NOZEMA', 'KANAAL 49' and 'ZUID-HOLLAND TV') were continuing. At present, a temporary 'standby' Marconi transmitter is in use, but the final transmitter will be located at the PTT tower at Rotterdam-Waalhaven, with the aerials mounted at a height of 200 m ASL.

The Dutch publisher VNU and the Luxembourg television company CLT are launching the country's second commercial channel, RTL5, which will offer sport, films and 'adult' entertainment. This new service will originate in Luxembourg.
Germany: SW-3 is now showing a 'Wetterpanorama' after closedown for the benefit of tourists. The information covers many areas of southern Germany. A new private regional TV service called 'Schamoni-TV' is coming on-air soon in the Berlin area. The studios are located at the foot of the Alexanderplatz TV tower.
Austria: ORF-2 now shows a 'Wetterpanorama' programme during the morning.
Luxembourg: The Dudelange transmitter on channel E7 is currently operating with an ERP of 130 kW.
Switzerland: Only the SSR-1 (French language) network seems to show the FuBK test card at switch-on; the DRS and TSI networks show text pages (Text Vision). All three networks open at 0600 UTC without an opening sequence or identification logo, and switch straight to 'Euronews'. The same pictures are shown via the three networks with sound straight in the appropriate langauge, either French, German or Italian, depending on the network.
Sweden: SVT-1 has been showing colour bars with a special test transmission announcement. A PM5544 test pattern headed 'TV1' has been radiated, as well as the usual 'SVERIGE' PM5534.
Portugal: The new names for the Portuguese first and second networks are 'Canal 1' and 'TV-2' respectively.
Finland: MTV has launched a special news programme called 'Talousuutiset', which reports on various issues about the economy. It commenced in August, and is screened after the regular news on MTV-3 on Mondays at 1920 (local time) and on Tuesday to Friday at 2220 (local time). Local television broadcasts have commenced in Närpiö. They have also been available in Kristiinankaupunki from August 16th.
Slovakia Republic: The STV-1 transmitter at Bratislava/Kamzik is now using CCIR system B with 5.5 MHz sound spacing.
Poland: TVP-2 will commence using the PAL colour system from January 1st, 1994. There are many SECAM-only receivers still in existence, but the type of compensation for viewers with these sets has yet to be agreed.
Moldova: TV Moldova is relaying various satellite services at the following local times: 1000-1015: news from TRT (Wednesday and Friday Euronews); 1700-1715: News from TV5. The channel R3 transmitter at Chisinau/Straseni is reported to have an ERP of 800 kW!
Jordan: A teletext service has now been introduced.
Iraq: Iraq Television International plans to establish a DBS satellite service using Arabsat and Eutelsat transponders from the end of 1993. Coverage will extend to more than 35 countries in Asia and Europe.
Israel: The franchises for a commercial second network (Channel 2) have been awarded to three of the seven groups that tendered for the licence — after a wait of more than 15 years!. The proposed opening of Channel 2 is planned for October. Each franchise owner will be allocated two days per week for broadcasting, with Saturdays assigned to the three groups in rotation.
Samoa: The TV New Zealand Pacific Service and its transmission subsidiary BCL have helped establish 'Televise Samoa', which went on-air last May.

This month's service information was kindly supplied by Gösta van der Linden and the BDXC, Netherlands; Reflexion, Germany; Garry Smith, UK; Pertti Salonen, Finland; Roger Bunney, UK; Andrew Emmerson, UK; Thomas Pahlke, Germany; Bernd Trutenau, Lithuania.

Please send any news about DX-TV in your part of the world to: Keith Hamer, 7 Epping Close, Derby DE3 4HR, England.

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April 1993

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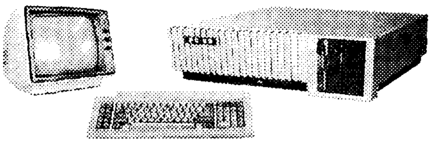

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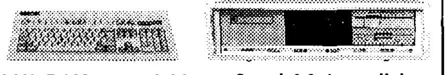

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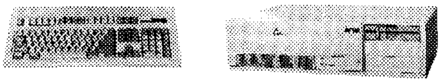

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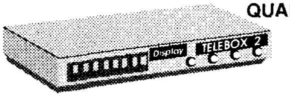

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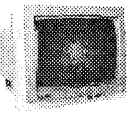

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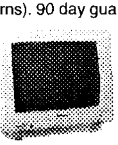

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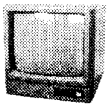

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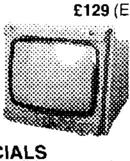

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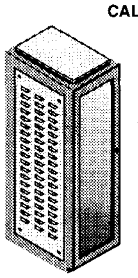

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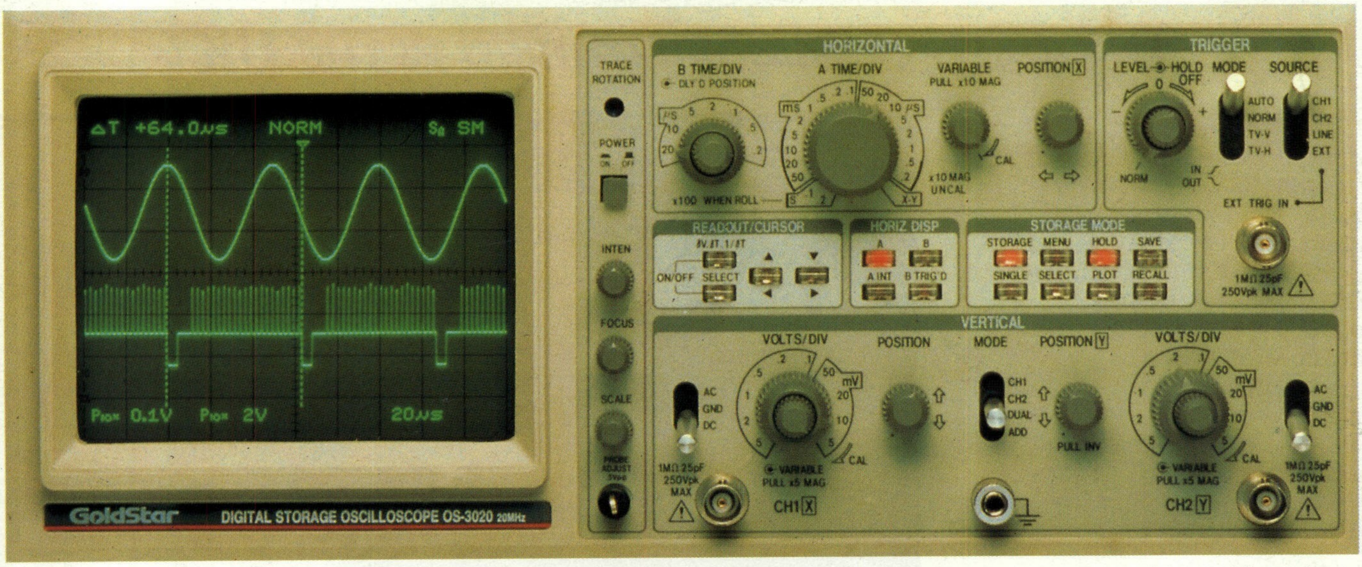

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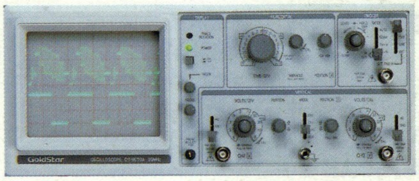

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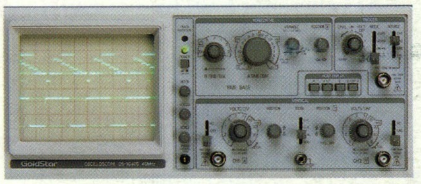

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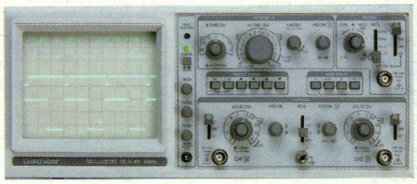
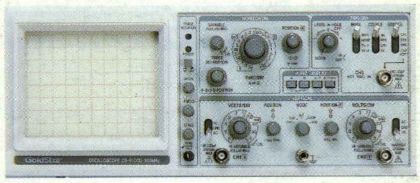
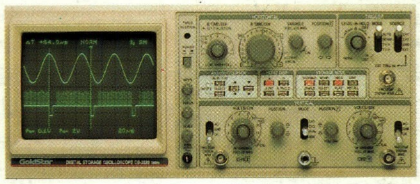


OS-904RD GW06G **£499.95**



OS-9100D GW05F **£699.95**



OS-3020 GW07H **£749.95**

All models are supplied complete with probes, mains lead, spare fuses and detailed operating manual. Full details and specifications can be found in the **1994 Maplin Full Colour Catalogue**, available from **WHSMITH** and selected branches of **RSMcColl** in Scotland for £2.95 (£3.45 by post direct from Maplin). To order, Phone the Credit Card Hotline, 0702 554161, or send your Mail Order to P.O Box 3, Rayleigh, SS6 2BR, or visit your local Maplin store. Please note latest models all now cream in colour as Model OS-3020.

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